

Publication List for MSLAB (1994-present)

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Books

- B1. Zhanhai Qin, Sheldon X.-D. Tan and Chung-Kuan Cheng, [Symbolic Analysis and Reduction of VLSI Circuits](#), Springer Publisher, 2005, ISBN: 0-387-23904-9; e-ISBN: 0-387-23905-7.
- B2. Sheldon X.-D. Tan and Lei He, [Advanced Model Order Reduction Techniques for VLSI Designs](#), Cambridge University Press, 2007, ISBN-13 978-0-521-86581-4, ISBN-10 0-521-86581.
- B3. Ruijing Shen, Sheldon X.-D. Tan and Hao Yu, [Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs](#), Springer Publisher, March 2012, ISBN-10: 1461407877.
- B4. Esteban Tlelo-Cuautle, Sheldon X.-D. Tan (Editors), [VLSI Design](#), InTech Open Access Publisher, January 2012, ISBN 978-953-307-884-7.
- B5. Guoyong Shi, Sheldon X.-D. Tan, Esteban Tlelo-Cuautle, “[Advanced Symbolic Analysis for VLSI Systems -- Methods and Applications](#)”, Springer Publisher, 2014, ISBN 978-1-4939-1103-5.
- B6. Sheldon X.-D. Tan, Mehdi Tahoori, Taeyoung Kim, Shengcheng Wang, Zeyu Sun and Saman Kiamehr, “[VLSI Systems Long-Term Reliability -- Modeling, Simulation and Optimization](#)”, Springer Publisher, 2019. DOI: 10.1007/978-3-030-26172-6, ISBN: 978-3-030-26171-9 (<https://www.springer.com/gp/book/9783030261719>).

Book Chapters:

- BC 1. C.-J. Shi and X.-D. Tan, “[Canonical Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams](#)” Part III and pp.344-361 in *Computer-Aided Design of Analog Integrated Circuit and Systems*, R. A. Rutenbar, G. E. Gielen and B. A. Antao (ed) , IEEE Press & [Wiley-Interscience](#), 2002. ISBN 0-471-22782-X.
- BC 2. Sheldon X.-D. Tan, Ruijing Shen, “Chip-Level Statistical Leakage Modeling and Analysis”, Chapter in *Recent Advancements in Modeling of Semiconductor Processes, Circuits and Chip-Level Interactions*, Rasit Onur Topaloglu, and Peng Li (Editors), Bentham Publishing (www.ebook-engineering.org), eISBN: 978-1-60805-074-1, Sept, 2011. ([online permanent address](#))
- BC 3. Sheldon X.-D. Tan, Esteban Tlelo-Cuautle, “Recent development in symbolic analysis: an overview”, Chapter in [Design of Analog Circuits through Symbolic Analysis](#), M. Fakhfakh, E. Tlelo-Cuautle and F.V. Fernández (Editors.), Bentham Science Publishers Ltd (www.ebook-engineering.org), ISBN: 9078-1-60805-095-6, 2012.
- BC 4. Sheldon X.-D. Tan, “Symbolic analysis by determinant decision diagrams and applications”, Chapter in [Design of Analog Circuits through Symbolic Analysis](#), M. Fakhfakh, E. Tlelo-Cuautle and F.V. Fernández (Editors.), Bentham Science Publishers Ltd (www.ebook-engineering.org), ISBN: 9078-1-60805-095-6, 2012.
- BC 5. Esteban Tlelo-Cuautle, Carlos Sanchez-Lopez, Elyoenai Martinez-Romero, Sheldon X.-D. Tan, Peng Li, Francisco Fernandez and Mourad Fakhfakh, “[Behavioral modeling of mixed-mode integrated circuits](#)”, Esteban Tlelo-Cuautle, Editor, Chapter in “[Advances in Analog Circuits](#)”, INTECH (www.intechweb.org), ISBN 978-953-307-323-1, Feb., 2011.
- BC 6. Xue-Xin Liu, Hao Yu, Hai Wang, Sheldon X.-D. Tan, “Analog mismatch analysis by stochastic nonlinear macromodeling”, Chapter in “[Analog Circuits: Applications, Design and Performances](#)”, E. Tlelo-Cuautle (Editor), NOVA Science Publishers Inc. ISBN: 978-1-61324-355-8. Sept., 2011
- BC 7. Sheldon X.-D. Tan, Xue-Xin Liu and Eric Mlinar, and Esteban Tlelo-Cuautle, “[Parallel symbolic analysis of large analog circuits on GPU platforms](#)”, Chapter 6 in “[VLSI Design](#)”, Esteban Tlelo-Cuautle and Sheldon X.-D. Tan (Editors), INTECH (www.intechweb.org), ISBN 978-953-307-884-7, January, 2012.
- BC 8. S. Rodriguez-Chavez, A.A. Palma-Rodriguez, E. Tlelo-Cuautle, and S. X.-D. Tan, “Graph-based symbolic and symbolic sensitivity analysis of analog integrated circuits”, Chapter in “*Analog/RF and Mixed-Signal Circuit Systematic Design*”, Mourad Fakhfakh, Esteban Tlelo-Cuautle, R. Castro-Lopez (editors), Springer, 2012. ISBN 978-3-642-36328-3.
- BC 9. X.-X. Liu, S. X.-D. Tan, H. Wang, and H. Yu, “GPU-accelerated envelope-following method”, Chapter 17 in “[Designing Scientific Applications on GPU](#)”,

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Raphael Couturier (Editor), CRC Press /Taylor & Francis Group, Nov. 2013.
ISBN 9781466571648.

- BC 10. Han Zhou, Z. Sun and S. Sadiqbatcha, S. X.-D. Tan, “EM lifetime constrained optimization for multi-segment power grid networks”, Chapter 15 in “*Dependable Embedder Systems*”, Springer Publisher, 2019.

Ph.D. Thesis

- D1. Sheldon X.-D. Tan, “[Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams](#)”, University of Iowa, 1999.

Ph.D. Student Theses

- D2. Junjie Yang, “Behavioral Modeling and Simulation of Analog Circuits”, University of California at Riverside, Dec.23, 2004.
- D3. Jeffrey Fan, “Process variation aware interconnect simulation and optimization in VLSI Design”, University of California at Riverside, May 8, 2007.
- D4. Hang Li, “Power and Thermal Integrity Analysis and Optimization for Nanometer VLSI System”, University of California at Riverside, May 18, 2007.
- D5. Wei Wu, “Power/Thermal Modeling and Dynamic Thermal Management for SRAM Structure”, University of California at Riverside, Feb. 15, 2008.
- D6. Pu Liu, “Advanced Model Reduction and Simulation Techniques for Integrated Electronic and Thermal Circuit”, University of California at Riverside, March. 3, 2008.
- D7. Boyuan Yan, “Advanced non-Krylov Subspace Model Order Reduction Techniques for Interconnect Circuits”, University of California at Riverside, Nov. 25, 2009.
- D8. Ning Mi, “Statistical Analysis for On-chip Power Grid Networks and Interconnects Considering Process Variation”, University of California at Riverside, Dec. 7, 2009.
- D9. Duo Li, “Modeling, Characterization and Simulation of On-Chip Power Delivery Networks and Temperature Profile on Multi-Core Microprocessors”, University of California at Riverside, September 15, 2010.
- D10. Ruijing Shen, “Statistical Performance Characterization and Analysis of Nano-Scale VLSI Circuits”, University of California at Riverside, Dec. 8, 2011.
- D11. Hai Wang, “Compact Modeling and Analysis for Electronic and Thermal Effects of Nanometer Integrated and Packaged Systems”, University of California at

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Riverside, April 10, 2012.

- D12. Zhigang Hao, “Computer-Aided Design Methods for Variational Analysis of Nanoscale Mixed-Signal Integrated Circuits”, co-advised with Prof. Guoyong Shi of SJTU. May, 2012 and he got Ph.D. from SJTU.
- D13. Xuexin Liu, “Parallel and Statistical Analysis and Modeling of Nanometer VLSI Systems”, University of California at Riverside, March 11, 2013.
- D14. Zao Liu, “System-level thermal modeling and management for multi-core and 3D microprocessors”, University of California at Riverside, May 9, 2014.
- D15. Kai He, “Parallel CAD algorithms and hardware security for VLSI Systems”, University of California at Riverside, July 29, 2016.
- D16. Xin Huang, “Physics-Based Electromigration and Time Dependent Dielectric Breakdown Modeling and Reliability Analysis for Nanometer VLSI Circuits”, University of California at Riverside, July 29, 2016.
- D17. Taeyoung Kim, “System-Level Electromigration-Induced Dynamic Reliability Management”, Dept. of Computer Science and Engineering, University of California at Riverside, June 1st, 2017.
- D18. Hengyang Zhao, “FEM Based Multi-physics Analysis of Electromigration Voiding Problems in Nanometer Integrated Circuits”, ECE, University of California at Riverside, Nov. 11, 2018
- D19. Chase Cook, “Simulation for Reliability, Hardware Security, and Ising Computing in VLSI Chip”, ECE, University of California at Riverside, Dec. 2019
- D20. Zeyu Sun, “Physics-Based Electromigration Modeling and Analysis and Optimization”, ECE, ECE, University of California at Riverside, March, 2020

Conference Presentations and Posters (informal publication).

- I1. Xuexin Liu, Kuangya Zhai, Sheldon X.-D. Tan, “Fast thermal analysis of 3D Integrated Circuits and CPU-GPU Platforms”, GPU Technology Conference, San Jose, March, 2013. (By Xuexin Liu).
- I2. S. Ahn, H. Y. Chiang, L. Suasnabar, S. X.-D. Tan, J. Zhou, “Practical high-speed network modeling and analysis”, Southern California Conference for Undergraduate Research (SCCUR), California State at Fullerton, Nov. 2014.
<https://apps.fullerton.edu/CSUFConferences/SCCUR/Submission/Status?submissionCode=83C6NhWC>
- I3. H. Zhao and S. X.-D. Tan, “A Finite element method for modeling void growth in

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electromigration Failure Process”, *International Integrated Reliability Workshop (IIRW), Fallen Leaf Lake, CA, 2017*. (Open poster)

- I4. Sheldon Tan, Sheriff Sadiqbatcha, “Fast EM-Aging Acceleration Techniques for sub10nm VLSI Interconnect”, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, Nov. 2018.

Tutorials:

- T1. Paul M. Harvey, Howard Chen, Chung-Kuan Cheng, Manjid Borah, Lei He, and Sheldon X.-D. Tan, "High Performance Interconnect and Packaging", full day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference*, January 24, 2006.
- T2. Sheldon X.-D. Tan, J. Fan, “Inductance Extraction and Compact Modeling of Inductively Coupled Interconnects in the Presence of Process Variations”, half-day tutorial, *IEEE ASICON’07*, Oct. 2007 (**invited**).
- T3. Sheldon X.-D. Tan, “Advanced modeling and analysis techniques for nanometer interconnect and multi-core VLSI circuits”, ASIC & System Lab, **Fudan University**, July 27 to Aug. 1, 2008. (Four presentations were given in the short course), Shanghai, China.
- T4. Sheldon X.-D. Tan and Hai Wang, “Architecture level thermal modeling, prediction and management for multi-core and 3D microprocessors”, a half day tutorial, *IEEE/ACM Asia South-Pacific Design Automation Conference*, Singapore, Singapore, January 24, 2014.
- T5. Valeriy Sukharev, Sheldon Tan, Marko Chew, “Full-chip Electromigration Assessment and System-level EM Reliability Management”, embedded tutorial, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, Nov. 2014.
- T6. Sheldon Tan, Medhi Tahoori, Haibao Chen, “Cross-Layer Reliability Aware Design, Optimization and Dynamic Management”, tutorial, *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Chiba, Japan, Jan. 2017
- T7. Sheldon Tan and Hussam Amrouch, “Design for Reliability in the Nano-CMOS Era: New Holistic Methodologies for Reliability Modeling and Optimization”, tutorial, *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, Jan. 2019

Patents:

- P1. Sheldon X.-D. Tan, X. Wang, B.A. Fairbanks, “[I/O Pin Placement Algorithm For Programmable Logic Devices](#)” Filed on May, 2003. U.S. Patent No. 7111265

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(approved on 9/19/2006).

- P2. Sheldon X.-D. Tan, B. Yan, “Decentralized complexity reduction of parasitic interconnect circuits”, UC Case No. 2008-783-1, US provisional patent. (filed on May 28, 2008)
- P3. Sheldon X.-D. Tan, D. Li, “Extended truncated balanced realization method for on-chip power grid network analysis”, UC Case No. 2008-784-1, US provisional patent. (filed on Feb. 27, 2008).
- P4. X. Hong, Y. Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, “Transient analysis of on-chip power grid networks based on equivalent circuits”, Patent No. ZL 03104770.X (China)
- P5. X. Hong, Y. Cai, J. Fu, Y. Luo, Z. Pan, Sheldon X.-D. Tan, “Fast decap allocation method for noise reduction in the on-chip power grid networks”, Patent No. ZL031570526 (China)
- P6. X. Hong, Y. Cai, Z. Pan, Y. Luo, J. Fu, Sheldon X.-D. Tan, “Relaxed hierarchical transient analysis method for power grid networks”, Patent No. ZL 200510011804.2 (China)
- P7. Sheldon X.-D. Tan, Kai Hem Xin Huang, “On-Chip Aging Sensor and Counterfeit Integrated Circuit Detection Method”, US patent No. 10298236 B3 (approved on May 21, 2019).

Preprint papers:

C. Cook, W. Jin and S. X.-D. Tan, “GPU-based Ising computing for solving balanced min-cut graph partitioning problem”, <https://arxiv.org/abs/1908.00210>

Journal Articles

- J1. X.-D. Tan, J.-R. Tong, and P.-S. Tang. "A general algorithm for multi-way digital circuit partitioning." *Chinese Journal of Electronics*, vol. 24, no. 8, 1996.
- J2. X.-D. Tan, J.-R. Tong, and P.-S. Tang. "A multiple-optimization algorithm for multiple way VLSI network partitioning," *Chinese Journal of Computers*, vol. 19, no. 5, 1996.
- J3. C.-J. Shi and X.-D. Tan. "[Canonical symbolic analysis of large analog circuits with determinant decision diagrams.](#)" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 1-18, 2000.
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- J7. X.-D. Tan and C.-J. Shi. "[Balanced multi-level multi-way partitioning of large analog integrated circuits for hierarchical symbolic analysis.](#)" *Integration, The VLSI Journal*, vol 34/1-2 pp 65 – 86, 2003.
- J8. X.-D. Tan, C.-J. Shi and F. J.-C. Lee. "[Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings.](#)", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. vol. 22, no. 12, pp. 1678-1684, Dec. 2003.
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- C150 J. Ma, H. Wang, S. X.-D. Tan, C. Zhang, H. Tang, "Hybrid dynamic thermal management method with model predictive control", *IEEE Asia Pacific Conference on Circuit and Systems (APCCAS'14)*, Ishigaki Island, Okinawa, Japan, Nov. 2014.
- C151 Y. Zhu, S. X.-D. Tan, "GPU-accelerated parallel Monte Carlo analysis of analog circuits by hierarchical graph-based solver", *Proc. Asia South Pacific Design Automation Conference (ASP-DAC'15)*, Chiba, Japan, Jan. 2015.
- C152 H. Chen, S. X.-D. Tan, X. Huang, V. Sukharev, "New electromigration modeling and analysis considering time-varying temperature and current densities", *Proc. Asia South Pacific Design Automation Conference (ASP-DAC'15)*, Chiba, Japan, Jan. 2015. **(Best Paper Award Nomination, 7 out of 318)**
- C153 H. Shin, S. X.-D. Tan, G. Shi and E. Tlelo-Cuautle, "Rare event diagnosis by iterative failure region locating and elite learning sample selection", *Latin-American Test Symposium (LATS)*, Puerto Vallarta, Mexico, March, 2015.
- C154 H. Chen, X. Huang, V. Sukharev, S. X.-D. Tan and T. Kim, "Interconnect reliability modeling and analysis for multi-branch interconnect trees", *Proc. IEEE/ACM Design Automation Conference (DAC'15)*, San Francisco, June, 2015.
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- C156 Y. Zhao, H. Shin, H. Chen, S. X.-D. Tan, G. Shi, X. Li, "Statistical rare event analysis using smart sampling and parameter guidance", *28th IEEE International SoC Conference (SOCC2015)*, Beijing, Sept, 2015.
- C157 X. Huang, V. Sukharev, J.-H. Choy, H. Chen, E. Tlelo-Cuautle and S. X.-D. Tan, "Full-chip electromigration assessment: effect of cross-layout temperature and thermal stress distributions", *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*,

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- C192 C. Cook, S. Sadiqbatcha. Z. Sun and S. X.-D. Tan, “Reliability based hardware trojan design based on physics-based electromigration models”, *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD’18), Prague, Czech Republic, July 2018.
- C193 H. Zhao and S. X.-D. Tan, “Multi-physics-based FEM analysis for post-voiding analysis of electromigration failure effects”, *Proc. IEEE/ACM International Conf. on Computer-Aided Design* (ICCAD’18), San Diego, CA, Nov. 2018. **(invited)**
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- C195 S. Sadiqbatcha, H. Zhao, H. Amrouch, J. Henkel and S. X.-D. Tan, "Hot spot identification and system parameterized thermal modeling for multi-core processors through infrared thermal imaging", *Proc. Design, Automation and Test in Europe* (DATE'19), Florence, Italy, March 2019.
- C196 Z. Sun, H. Zhou, and S. X.-D. Tan, “Dynamic reliability management for multi-core processor based on deep reinforcement learning”, *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD’19), Lausanne, Switzerland, July 2019.
- C197 Z. Sun, T. Kim, M. Chow, S. Peng, H. Zhou, H. Kim, D. Wong and S. X.-D. Tan, “Long-term reliability management for multitasking GPGPUs”, *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD’19), Lausanne, Switzerland, July 2019.
- C198 K. Yang, S. Peng, S. X.-D. Tan, and H. Chen. “Multi-thread assembling for fast FEM power delivery DC Integrity Analysis”. *IEEE 13th International Conference on ASIC* (ASICON), Oct. 2019
- C199 S. Sadiqbatcha, Y. Zhao, J. Zhang, H. Amrouch, J. Henkel and S. X.-D. Tan, "Machine learning based online full-chip heatmap estimation," *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC’20), Beijing, China, Jan. 2020.
- C200 H. Zhou, S. Yu, Z. Sun, and S. X.-D. Tan, “Reliable power grid network design framework considering EM mortalities for multi-segment wires”, *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC’20), Beijing, China, Jan. 2020. **(Invited)**
- C201 S. Ma, X. Wang, S. X.-D. Tan, L. Chen and J. He, “An adaptive electromigration assessment algorithm for full-chip power/ground networks”, *Proc. Asia South Pacific Design Automation Conference* (ASP-DAC’20), Beijing, China, Jan. 2020.

- C202 J. Zhang, S. Sadiqbatcha, W. Jin and S. X.-D. Tan, “Accurate power density map estimation for commercial multi-core microprocessors”, *Proc. Design, Automation and Test in Europe (DATE’20)*, Grenoble, France, March 2020.
- C203 S. Yu, H. Zhou, H. Amrouch, J. Henkel, S. X.-D. Tan, “Run-time accuracy reconfigurable stochastic computing for dynamic reliability and power management: work-in-progress”, *Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES’20)*, ESWeek 2020, Sept 2020.
- C204 H. Zhou, W. Jin, and S. X.-D. Tan, “GridNet: Fast date-driven EM-induced IR drop prediction and localized fixing for on-chip power grid networks”, *Proc. IEEE/ACM International Conf. on Computer-Aided Design (ICCAD’18)*, San Diego, CA, Nov. 2020. (23.8% acceptance rate)
- C205 M. Kavousi, L. Chen, and S. X.-D. Tan, “Electromigration immortality check considering Joule heating effect of multi-segment wires”, *Proc. IEEE/ACM International Conf. on Computer-Aided Design (ICCAD’18)*, San Diego, CA, Nov. 2020. (23.8% acceptance rate)
- C206 W. Jin, S. Sadiqbatcha, J. Zhang and S. X.-D. Tan, “Full-chip thermal map estimation for multi-core commercial CPUs with generative adversarial learning”, *Proc. IEEE/ACM International Conf. on Computer-Aided Design (ICCAD’18)*, San Diego, CA, Nov. 2020. (invited)

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- Arx2. Shaoyi Peng and Sheldon X.-D. Tan. “GLU3.0: Fast GPU-based Parallel Sparse LU Factorization for Circuit Simulation.” <https://arxiv.org/abs/1908.00204>
- Arx3. Chase Cook, Wentian Jin and Sheldon X.-D. Tan, “GPU-based Ising computing for solving balanced min-cut graph partitioning problem”, <https://arxiv.org/abs/1908.00210>
- Arx4. Tan, Sheldon X.-D. and Liang Chen. “Real-Time Differential Epidemic Analysis and Prediction for COVID-19 Pandemic.” <https://arxiv.org/abs/2004.06888>
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- Arx6. Yu, Shuyuan, Han Zhou, Shaoyi Peng, Hussam Amrouch, Jörg Henkel and Sheldon X.-D. Tan. “Run-Time Accuracy Reconfigurable Stochastic Computing for Dynamic Reliability and Power Management.” <https://arxiv.org/abs/2004.13320>

Publication List of MSLAB

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