

Advanced Model Order Reduction Techniques in VLSI Design

Model order reduction (MOR) techniques are important in reducing the complexity of nanometer VLSI designs, and consequently controlling “parasitic” electromagnetic effects, so that higher operating speeds and smaller feature sizes can be achieved. This book presents a systematic introduction to, and treatment of, the key MOR methods used in general linear circuits, using real-world examples to illustrate the advantages and disadvantages of each algorithm.

Starting with a review of traditional projection-based techniques and proofs of some fundamental theories, coverage progresses to advanced “state-of-the-art” MOR methods for VLSI design. These include HMOR, passive truncated balanced realization (TBR) methods, efficient inductance modeling via the VPEC model, general model optimization and passivity enforcement methods, passive model realization techniques, and structure-preserving MOR techniques. Numerical methods have been used throughout, and, where possible, approached from the CAD engineer’s perspective. This avoids complex mathematics, and allows the reader to take on real design problems and develop more effective tools.

With practical examples and over 100 illustrations, this book is suitable for researchers and graduate students of electrical and computer engineering, as well as for practitioners working in the VLSI design and design automation industries.

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CAMBRIDGE
UNIVERSITY PRESS
www.cambridge.org



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Cover designed by Hart McLeod

PRINTED IN THE UNITED KINGDOM

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