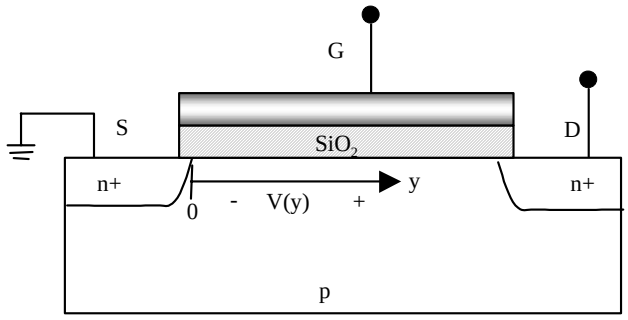
1. Consider a MOS capacitor with 10 nm of SiO_2 and Al metal on a 10 Ω cm p-type Si wafer. At the Si / SiO_2 interface there is a surface state charge of 10^{11} charges / cm^2. Using the δ-depletion approximation and values from Sze (specifically Fig. 21 p. 32, Fig. 4 p. 251, and App. H), find
(a) the metal semiconductor work function difference ϕ_{ms}.
(b) the flat band voltage, V_{FB}, which is defined as the gate voltage required to make the bands in the semiconductor flat, i.e. the surface potential is 0 (assuming the substrate is grounded).
(c) The surface potential at the onset of inversion
(d) The threshold voltage, V_T.
(e) The maximum depletion width, W_T.
(f) The electron and hole concentrations at the surface when the surface potential, ϕ_s equals 0, ϕ_f, and $2\phi_f$.
(g) What is the minimum high-frequency capacitance (see fig. 2.29 of Taur).

2. Consider an NMOSFET with a polysilicon (poly) gate (instead of metal). The poly is heavily doped poly-crystalline Si. For p-type poly, assume that in the poly, $E_f = E_v$, and for n-type poly, assume that $E_f = E_c$ (see Fig. 2.30 of Taur). For the electrostatic calculations, you can treat the poly as a metal, i.e. there is no voltage drop in the poly. The thickness of the SiO_2 is 10 nm and it is grown on a 10 Ω cm p-type Si wafer. At the Si / SiO_2 interface there is a surface state charge of 10^{11} charges / cm^2. i.e. everything is the same as in problem 2, except we have replaced the Al gate by heavily doped poly-Si.
(a) Calculate the threshold voltage for an n-type poly gate.
(b) Calculate the threshold voltage for an p-type poly gate.

3. For an NMOS FET we write that the electron charge per unit area under the gate is $Q_n(y) = Cox[V_{GS} - V(y) - V_t]$. Using the same approach that we used to derive the "square law" for I_D, derive an expression for the potential V(y) and the electric field component $E_y(y)$ in saturation.



4. For an npn BJT at T=300K with a base width of 0.05 μm and a minority electron mobility in the base of 800 cm^2/Vs, what is the maximum value for the transition frequency, f_T?

5. For an NMOS FET with μ_n in the channel equal to 800 cm^2/Vs, a gate length of 0.18 μm, and $(V_{GS} - V_t) = 0.4V$ what is the maximum value for the transition frequency, f_T, assuming the "square law" relation for I_D.