CHAPTER 4: Capacitance Modeling

Accurate modeling of MOSFET capacitance plays equally important role as that of the DC model. This chapter describes the methodology and device physics considered in both intrinsic and extrinsic capacitance modeling in BSIM3v3.2.2. Detailed model equations are given in Appendix B. One of the important features of BSIM3v3.2 is introduction of a new intrinsic capacitance model (capMod=3 as the default model), considering the finite charge thickness determined by quantum effect, which becomes more important for thinner T_{ox} CMOS technologies. This model is smooth, continuous and accurate throughout all operating regions.

4.1 General Description of Capacitance Modeling

BSIM3v3.2.2 models capacitance with the following general features:

- Separate effective channel length and width are used for capacitance models.
- The intrinsic capacitance models, capMod=0 and 1, use piece-wise equations. capMod=2 and 3 are smooth and single equation models; therefore both charge and capacitance are continous and smooth over all regions.
- Threshold voltage is consistent with DC part except for capMod=0, where a long-channel V_{th} is used. Therefore, those effects such as body bias, short/narrow channel and DIBL effects are explicitly considered in capMod=1, 2, and 3.
- Overlap capacitance comprises two parts: (1) a bias-independent component which models the effective overlap capacitance between the gate and the heavily doped source/drain; (2) a gate-bias dependent component between the gate and the lightly doped source/drain region.

- Bias-independent fringing capacitances are added between the gate and source as well as the gate and drain.

Name	Function	Default	Unit
capMod	Flag for capacitance models	3	(True)
vfbcv	the flat-band voltage for capMod = 0	-1.0	(V)
acde	Exponential coefficient for X_{DC} for accumulation and depletion regions	1	(m/V)
moin	Coefficient for the surface potential	15	($V^{0.5}$)
cgso	Non-LDD region G/S overlap C per channel length	Calculated	F/m
cgdo	Non-LDD region G/D overlap C per channel length	Calculated	F/m
CGS1	Lightly-doped source to gate overlap capacitance	0	(F/m)
CGD1	Lightly-doped drain to gate overlap capacitance	0	(F/m)
CKAPPA	Coefficient for lightly-doped overlap capacitance	0.6	
CF	Fringing field capacitance	equation (4.5.1)	(F/m)
CLC	Constant term for short channel model	0.1	μm
CLE	Exponential term for short channel model	0.6	
DWC	Long channel gate capacitance width offset	Wint	μm
DLC	Long channel gate capacitance length offset	Lint	μm

Table 4-1. Model parameters in capacitance models.

4.2 Geometry Definition for C-V Modeling

For capacitance modeling, MOSFET's can be divided into two regions: intrinsic and extrinsic. The intrinsic capacitance is associated with the region between the metallurgical source and drain junction, which is defined by the effective length

(L_{active}) and width (W_{active}) when the gate to S/D region is at flat band voltage. $L_{active}$and W_{active} are defined by Eqs. (4.2.1) through (4.2.4).

$$L_{active} = L_{drawn} - 2\delta L_{eff} \tag{4.2.1}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff} \tag{4.2.2}$$

$$\delta L_{eff} = DLC + \frac{Llc}{L^{\mathrm{Lln}}} + \frac{Lwc}{W^{Lwn}} + \frac{Lwlc}{L^{\mathrm{Lln}} W^{Lwn}} \tag{4.2.3}$$

$$\delta W_{eff} = DWC + \frac{Wlc}{L^{\mathrm{Wln}}} + \frac{Wwc}{W^{Wwn}} + \frac{Wwlc}{L^{\mathrm{Wln}} W^{Wwn}} \tag{4.2.4}$$

The meanings of *DWC* and *DLC* are different from those of *Wint* and *Lint* in the I-V model. L_{active} and W_{active} are the effective length and width of the intrinsic device for capacitance calculations. Unlike the case with I-V, we assumed that these dimensions have no voltage bias dependence. The parameter δL_{eff} is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate printing, etching and oxidation) on one side. Overall, a distinction should be made between the effective channel length extracted from the capacitance measurement and from the I-V measurement.

Traditionally, the L_{eff} extracted during I-V model characterization is used to gauge a technology. However this L_{eff} does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation. This L_{eff} is therefore very sensitive to the I-V equations used and also to the conduction characteristics of the LDD

region relative to the channel region. A device with a large L_{eff} and a small parasitic resistance can have a similar current drive as another with a smaller L_{eff} but larger R_{ds}. In some cases L_{eff} can be larger than the polysilicon gate length giving L_{eff} a dubious physical meaning.

The L_{active} parameter extracted from the capacitance method is a closer representation of the metallurgical junction length (physical length). Due to the graded source/ drain junction profile the source to drain length can have a very strong bias dependence. We therefore define L_{active} to be that measured at gate to source/drain flat band voltage. If *DWC*, *DLC* and the newly-introduced length/ width dependence parameters (*Llc*, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc*) are not specified in technology files, BSIM3v3.2.2 assumes that the DC bias-independent L_{eff} and W_{eff} (Eqs. (2.8.1) - (2.8.4)) will be used for C-V modeling, and *DWC*, *DLC*,*Llc*, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc* will be set equal to the values of their DC counterparts (default values).

4.3 Methodology for Intrinsic Capacitance Modeling

4.3.1 Basic Formulation

To ensure charge conservation, terminal charges instead of the terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain termianls, respectively. The gate charge is comprised of mirror charges from these components: the channel inversion charge (Q_{inv}), accumulation charge (Q_{acc}) and the substrate depletion charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate while the channel charge comes from the source and drain terminals

(4.3.1)

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases}$$

The substrate charge can be divided into two components - the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (δQ_{sub}). Q_g now becomes

(4.3.2)

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub}\right)$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by

(4.3.3)

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y$$

(4.3.4)

$$\begin{cases} Q_c = W_{active}\int_0^{L_{active}} q_c dy = -W_{active}C_{ox}\int_0^{L_{active}}\left(V_{gt} - A_{bulk}V_y\right)dy \\ Q_g = W_{active}\int_0^{L_{active}} q_g dy = W_{active}C_{ox}\int_0^{L_{active}}\left(V_{gt} + V_{th} - V_{FB} - \Phi_s - V_y\right)dy \\ Q_b = W_{active}\int_0^{L_{active}} q_b dy = -W_{active}C_{ox}\int_0^{L_{active}}\left(V_{th} - V_{FB} - \Phi_s + \left(A_{bulk} - 1\right)V_y\right)dy \end{cases}$$

Substituting the following

$$dy = \frac{dV_y}{\varepsilon_y}$$

and

$$I_{ds} = \frac{W_{active}\mu_{eff}C_{ox}}{L_{active}}\left(V_{gt} - \frac{A_{bulk}}{2}V_{ds}\right)V_{ds} = W_{active}\mu_{eff}C_{ox}\left(V_{gt} - A_{bulk}V_y\right)E_y \tag{4.3.5}$$

into Eq. (4.3.4), we have the following upon integration

$$\begin{cases} Q_c = -W_{active}\,L_{active}\,C_{ox}\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds} + \dfrac{{A_{bulk}}^2{V_{ds}}^2}{12\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds}\right)}\right) \\ Q_g = -Q_{sub\,0} + W_{active}\,L_{active}\,C_{ox}\left(V_{gt} - \dfrac{V_{ds}}{2} + \dfrac{A_{bulk}{V_{ds}}^2}{12\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds}\right)}\right) \\ Q_b = -Q_g - Q_c = Q_{sub} + Q_{sub\,0} + Q_{acc} \end{cases} \tag{4.3.6}$$

where

(4.3.7)

$$\begin{cases} Q_{sub\,0} = -W_{active} L_{active} \sqrt{2\varepsilon_{si} q N_{sub} (2\Phi_B - V_{bs})} \\ \delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\dfrac{1 - A_{bulk}}{2} V_{ds} + \dfrac{A_{bulk}(A_{bulk} - 1) V_{ds}^2}{12\left(V_{gt} - \dfrac{A_{bulk}}{2} V_{ds}\right)} \right) \end{cases}$$

The inversion charges are supplied from the source and drain electrodes such that $Q_{inv} = Q_s + Q_d$. The ratio of Q_d and Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 0, 0.5 and 1) which are the ratios of Q_d to Q_s in the saturation region. We will revisit charge partitioning in Section 4.3.4.

All capacitances are derived from the charges to ensure charge conservation. Since there are four terminals, there are altogether 16 components. For each component

(4.3.8)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where *i* and *j* denote the transistor terminals. In addition

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

4.3.2 Short Channel Model

In deriving the long channel charge model, mobility is assumed to be constant with no velocity saturation. Therefore in saturation region ($V_{ds} \geq V_{dsat}$), the carrier density at the drain end is zero. Since no channel length modulation is assumed, the channel charge will remain a constant throughout the saturation region. In essence, the channel charge in the

saturation region is assumed to be zero. This is a good approximation for long channel devices but fails when $L_{eff} < 2$ μm. If we define a drain bias, $V_{dsat,cv}$, in which the channel charge becomes a constant, we will find that $V_{dsat,cv}$ in general is larger than V_{dsat} but smaller than the long channel V_{dsat}, given by V_{gt}/A_{bulk}. However, in old long channel charge models, $V_{dsat,cv}$ is set to V_{gt}/A_{bulk} independent of channel length. Consequently, C_{ij}/L_{eff} has no channel length dependence (Eqs. (4.3.6), (4.37)). A pseudo short channel modification from the long channel has been used in the past. It involved the parameter A_{bulk} in the capacitance model which was redefined to be equal to V_{gt}/V_{dsat}, thereby equating $V_{dsat,cv}$ and V_{dsat}. This overestimated the effect of velocity saturation and resulted in a smaller channel capacitance.

The difficulty in developing a short channel model lies in calculating the charge in the saturation region. Although current continuity stipulates that the charge density in the saturation region is almost constant, it is difficult to calculate accurately the length of the saturation region. Moreover, due to the exponentially increasing lateral electric field, most of the charge in the saturation region are not controlled by the gate electrode. However, one would expect that the total charge in the channel will exponentially decrease with drain bias. Experimentally,

$$V_{dsat,iv} < V_{dsat,cv} < V_{dsat,iv}\Big|_{L_{active}\to\infty} = \frac{V_{gsteff,cv}}{A_{bulk}} \tag{4.3.9}$$

and $V_{dsat,cv}$ is modeled by the following

(4.3.10a)

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right)}$$

(4.3.10b)

$$V_{gsteff,cv} = noff \cdot nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}-voffcv}{noff \cdot nv_t}\right)\right)$$

Parameters *noff* and *voffcv* are introduced to better fit measured data above subthreshold regions. The parameter A_{bulk} is substituted A_{bulk0} in the long channel equation by

(4.3.11)

$$A_{bulk}' = A_{bulk0}\left(1+\left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right)$$

(4.3.11a)

$$A_{bulk} = \left(1+\frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_0}{W_{eff}'+B_1}\right)\right)\cdot\frac{1}{1+KetaV_{bseff}}$$

In (4.3.11), parameters *CLC* and *CLE* are introduced to consider channel-length modulation.

4.3.3 Single Equation Formulation

Traditional MOSFET SPICE capacitance models use piece-wise equations. This can result in discontinuities and non-smoothness at transition regions. The following describes single-equation formulation for charge, capacitance and voltage modeling in capMod=2 and 3.

(a) Transition from depletion to inversion region

The biggest discontinuity is the inversion capacitance at threshold voltage. Conventional models use step functions and the inversion capacitance changes abruptly from 0 to C_{ox}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to 0 at threshold voltage. Both of these effects can cause oscillation during circuit simulation. Experimentally, capacitance starts to increase almost quadratically at ~0.2V below threshold voltage and levels off at ~0.3V above threshold voltage. For analog and low power circuits, an accurate capacitance model around the threshold voltage is very important.

The non-abrupt channel inversion capacitance and substrate capacitance model is developed from the I-V model which uses a single equation to formulate the subthreshold, transition and inversion regions. The new channel inversion charge model can be modified to any charge model by substituting V_{gt} with $V_{gsteff,cv}$ as in the following

$$Q\left(_{Vgt}\right) = Q\left(V_{gsteff,CV}\right) \tag{4.3.12}$$

Capacitance now becomes

(4.3.13)

$$C(V_{gt}) = C(V_{gsteff,CV})\frac{\partial V_{gsteff,CV}}{V_{gs,ds,bs}}$$

The "inversion" charge is always non-zero, even in the accumulation region. However, it decreases exponentially with gate bias in the subthreshold region.

(b) Transition from accumulation to depletion region

An effective flatband voltage V_{FBeff} is used to smooth out the transition between accumulation and depletion regions. It affects the accumulation and depletion charges

(4.3.14)

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3^2 + 4\delta_3 vfb}\right\} \quad where\, V_3 = vfb - V_{gs} + V_{bseff} - \delta_3;\ \delta_3 = 0.02V$$

(4.3.15)

$$vfb = V_{th} - \Phi_s - K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

In BSIM3v3.2.2, a bias-independent V_{th} is used to calculate *vfb* for capMod = 1, 2 and 3. For capMod = 0, *Vfbcv* is used instead (refer to the appendices).

(4.3.16)

$$Q_{acc} = -W_{active} L_{active} C_{ox}\left(V_{FBeff} - vfb\right)$$

(4.3.17)

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \cdot \frac{K_{1ox}^2}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff}\right)}{K_{1ox}^2}}\right)$$

(c) Transition from linear to saturation region

An effective V_{ds}, V_{cveff}, is used to smooth out the transition between linear and saturation regions. It affects the inversion charge.

(4.3.18)

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat,cv}}\right\} \quad where V_4 = V_{dsat,cv} - V_{ds} - \delta_4;\ \delta_4 = 0.02V$$

(4.3.19)

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left(\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right) + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(4.3.20)

$$\delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}') A_{bulk}' V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

Below is a list of all the three partitioning schemes for the inversion charge:

(i) The 50/50 charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain nodes.

(4.3.21)

$$Q_s = Q_d = 0.5Q_{inv} = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

(ii) The 40/60 channel-charge partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain terminals by assuming a linear dependence on the position *y*.

(4.3.22)

$$\begin{cases} Q_s = W_{active}\int_0^{L_{active}} q_c\left(1 - \frac{y}{L_{active}}\right)dy \\ Q_d = W_{active}\int_0^{L_{active}} q_c\frac{y}{L_{active}}dy \end{cases}$$

(4.3.23)

$$Qs = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffCV}^3 - \frac{4}{3}V_{gsteffCV}^2 A_{bulk}'V_{cveff} + \frac{2}{3}V_{gsteffCV}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(4.3.24)

$$Q_d = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{5}{3}V_{gsteffcv}^2\left(A_{bulk}'V_{cveff}\right) + V_{gsteffcv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(iii) The 0/100 Charge Partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion

charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,c}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{\left(A_{bulk}' V_{cveff}\right)^2}{24\left(V_{gsteff,c} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.25}$$

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,c}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{\left(A_{bulk}' V_{cveff}\right)^2}{8\left(V_{gsteff,c} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.26}$$

(d) Bias-dependent threshold voltage effects on capacitance

Consistent Vth between DC and CV is important for acurate circuit simulation. capMod=1, 2 and 3 use the same Vth as in the DC model. Therefore, those effects, such as body bias, DIBL and short-channel effects are all explicitly considered in capacitance modeling. In deriving the capacitances additional differentiations are needed to account for the dependence of threshold voltage on drain and substrate biases.

4.4 Charge-Thickness Capacitance Model

Current MOSFET models in SPICE generally overestimate the intrinsic capacitance and usually are not smooth at V_{fb} and V_{th}. The discrepancy is more

pronounced in thinner T_{ox} devices due to the assumption of inversion and accumulation charge being located at the interface. The charge sheet model or the band-gap(E_g)-reduction model of quantum effect [31] improves the Φ_B and thus the V_{th} modeling but is inadequate for CV because they assume zero charge thickness. Numerical quantum simulation results in Figure 4-1 indicate the significant charge thickness in all regions of the CV curves [32].

This section describes the concepts used in the charge-thichness model (CTM). Appendix B lists all charge equations. A full report and anaylsis of the CTM model can be found in [32].

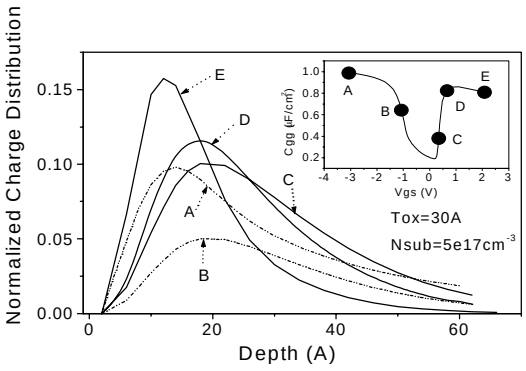

Figure 4-1. Charge distribution from numerical quantum simulations show significant charge thickness at various bias conditions shown in the inset.

CTM is a charge-based model and therefore starts with the DC charge thicknss, X_{DC}. The charge thicknss introduces a capacitance in series with C_{ox} as illustrated in Figure 4-2, resulting in an effective C_{ox}, C_{oxeff}. Based on numerical self-consistent solution of Shrodinger, Poisson and Fermi-Dirac equations, universal and analytical X_{DC} models have been developed. C_{oxeff} can be expressed as

(4.4.1)

$$C_{oxeff} = \frac{C_{ox}C_{cen}}{C_{ox} + C_{cen}}$$

where

$$C_{cen} = \varepsilon_{si} / X_{DC}$$

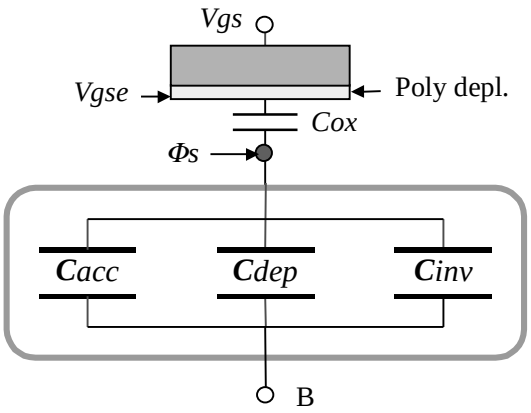

Figure 4-2. Charge-thickness capacitance concept in CTM. V_{gse} accounts for the poly depletion effect.

(i) X_{DC} for accumulation and depletion

The DC charge thickness in the accumulation and depletion regions can be expressed by [32]

(4.4.2)

$$X_{DC} = \frac{1}{3} L_{debye} \exp\left[acde \cdot \left(\frac{N_{sub}}{2\times 10^{16}} \right)^{-0.25} \cdot \frac{V_{gs} - V_{bs} - V_{fb}}{T_{ox}} \right]$$

where X_{DC} is in the unit of cm and (V_{gs} - V_{bs} - *vfb*) / T_{ox} has a unit of MV/cm. The model parameter *acde* is introduced for better fitting with a default value of 1. For numerical statbility, (4.4.2) is replaced by (4.4.3)

$$X_{DC} = X_{\max} - \frac{1}{2}\left(X_0 + \sqrt{X_0^2 + 4\delta_x X_{\max}}\right) \tag{4.4.3}$$

where

$$X_0 = X_{\max} - X_{DC} - \delta_x$$

and $X_{max}=L_{debye}/3$; $\delta_x = 10^{-3}T_{ox}$.

(ii) X_{DC} of inversion charge

The inversion charge layer thichness [32] can be formulated as

$$X_{DC} = \frac{1.9\times10^{-7}}{1+\left(\frac{V_{gsteff}+4(V_{th}-vfb-2\Phi_B)}{2T_{ox}}\right)^{0.7}} \quad [cm] \tag{4.4.4}$$

Through *vfb* in (4.3.30), this equation is found to be applicable to N^+ or P^+ poly-Si gates as well as other future gate materials. Figure 4-3 illustrates the universality of (4.3.30) as verified by the numerical quantum simulations, where the *x*-axe

represents the boundary conditions (the average of the electric fields at the top and the bottom of the charge layers) of the Schrodinger and the Poisson equations.

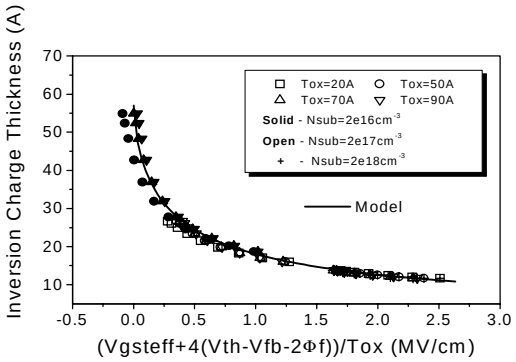

Figure 4-3. For all T_{ox} and N_{sub}, modeled inversion charge thickness agrees with numerical quantum simulations.

(iii) Body charge thichness in inversion

In inversion region, the body charge thickness effect is accurately modeled by including the deviation of the surface potential Φ_s from $2\Phi_B$ [32]

$$\Phi_\delta = \Phi_s - 2\Phi_B = v_t \ln\left(\frac{V_{gsteff,cv}\cdot\left(V_{gsteff,cv}+2K_{1ox}\sqrt{2\Phi_B}\right)}{moin\,K_{1ox}v_t^2}+1\right) \tag{4.4.5}$$

where the model parameter *moin* (defaulting to 15) is introduced for better fit to different technologies. The inversion channel charge density is therefore derived as

$$q_{inv} = -C_{oxeff}\cdot\left(V_{gsteff,cv}-\Phi_\delta\right) \tag{4.4.6}$$

Figure 4-4 illustrates the universality of CTM model by compariing C_{gg} of a SiON/ Ta_2O_5/TiN gate stack structure with an equivalent T_{ox} of 1.8nm between data, numerical quantum simulation and modeling [32].

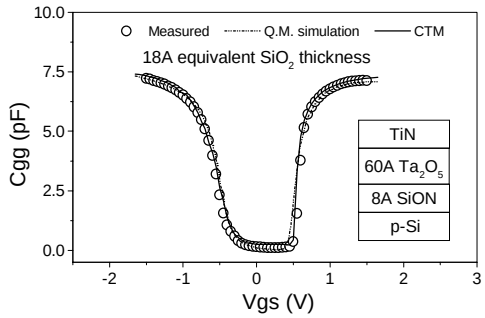

Figure 4-4. Universality of CTM is demonstrated by modeling the C_{gg} of 1.8nm equivalent T_{ox} NMOSFET with SiON/Ta_2O_5/TiN gate stack.

4.5 Extrinsic Capacitance

4.5.1 Fringing Capacitance

The fringing capacitance consists of a bias independent outer fringing capacitance and a bias dependent inner fringing capacitance. Only the bias independent outer fringing capacitance is implemented. Experimentally, it is virtually impossible to separate this capacitance with the overlap capacitance. Nonetheless, the outer fringing capacitance can be theoretically calculated by

(4.5.1)

$$CF = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{t_{poly}}{T_{ox}}\right)$$

where t_{poly} is equal to 4×10^{-7} m. *CF* is a model parameter.

4.5.2 Overlap Capacitance

An accurate model for the overlap capacitance is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small, we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap}$ = $C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

(i) Source Overlap Charge

(4.5.2)

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0 \cdot V_{gs} + CGS1\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPA}{2}\left(-1 + \sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPA}}\right)\right)$$

(4.5.3)

$$V_{gs,overlap} = \frac{1}{2}\left(V_{gs} + \delta_1 - \sqrt{\left(V_{gs} + \delta_1\right)^2 + 4\delta_1} \right), \quad \delta_1 = 0.02V$$

where *CKAPPA* is a model parameter. *CKAPPA* is related to the average doping of LDD region by

$$CKAPPA = \frac{2\varepsilon_{si} q N_{LDD}}{C_{ox}^{\ 2}}$$

The typical value for N_{LDD} is 5×10^{17} cm^{-3}.

(ii) Drain Overlap Charge

(4.5.4)

$$\frac{Q_{overlap,d}}{W_{active}} = CGD0 \cdot V_{gd} + CGD1\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPA}{2}\left(-1 + \sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPA}} \right) \right)$$

(4.5.5)

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd} + \delta_1 - \sqrt{\left(V_{gd} + \delta_1\right)^2 + 4\delta_1} \right), \quad \delta_1 = 0.02V$$

(iii) Gate Overlap Charge

(4.5.6)

$$Q_{overlap,g} = -\left(Q_{overlap,d} + Q_{overlap,s} + \left(CGB0 \cdot L_{active}\right) \cdot V_{gb}\right)$$

In the above expressions, if *CGS*0 and *CGD*0 (the overlap capacitances between the gate and the heavily doped source/drain regions, respectively) are not given, they are calculated according to the following

*CGS*0 = (*DLC***C*$_{ox}$) - *CGS*1 (if *DLC* is given and *DLC* > *0*)

*CGS*0 = 0 (if the previously calculated *CGS*0 is less than 0)

*CGS*0 = 0.6 $Xj*C_{ox}$ (otherwise)

*CGD*0 = ($DLC*C_{ox}$) - *CGD*1 (if *DLC* is given and *DLC* > *CGD*1/*Cox*)

*CGD*0 = 0 (if previously calculated *CDG*0 is less than 0)

*CGD*0 = 0.6 $Xj*C_{ox}$ (otherwise).

*CGB*0 in Eqn. (4.5.6) is a model parameter, which represents the gate-to-body overlap capacitance per unit channel length.