Digital Integrated Circuit (IC) Layout and Design - Lecture 4

- **FIRST LAB this Friday Jan. 20 (tomorrow)**
- 2 Lab sections
  - M 2:10pm – 5pm ENGR2 128
  - F 11:10am – 2pm ENGR2 128

http://www.ee.ucr.edu/~rlake/EE134.html

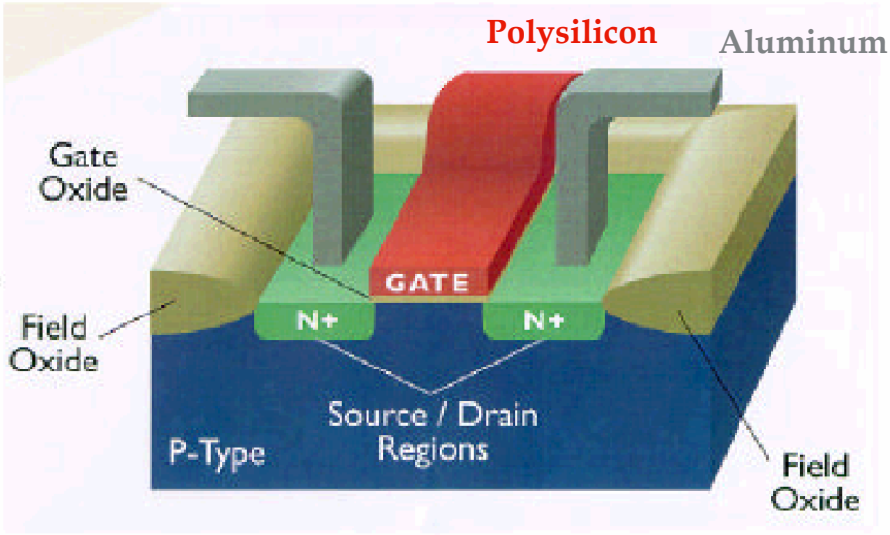
Reading and Prelab

- **Week 1**
  - Read Chapter 1 of text.
- **Week 2**
  - Read Chapter 2 of text.
- **Prelab**
  - Read insert A of text, pp. 67 - 71.
  - The lab will make more sense if you read this before lab.
  - There is nothing to turn in.

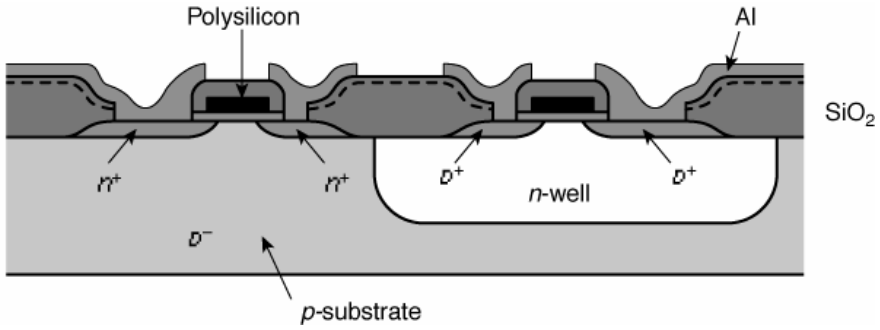
Agenda

- **Last Lecture**
  - MOS manufacturing process
  - Design rules
- **Today's Lecture**
  - MOS manufacturing process
  - Design rules
  - Layout and Design
  - Ties to V_{DD} and GND
  - Padframes
  - Pin Packages

The MOS Transistor

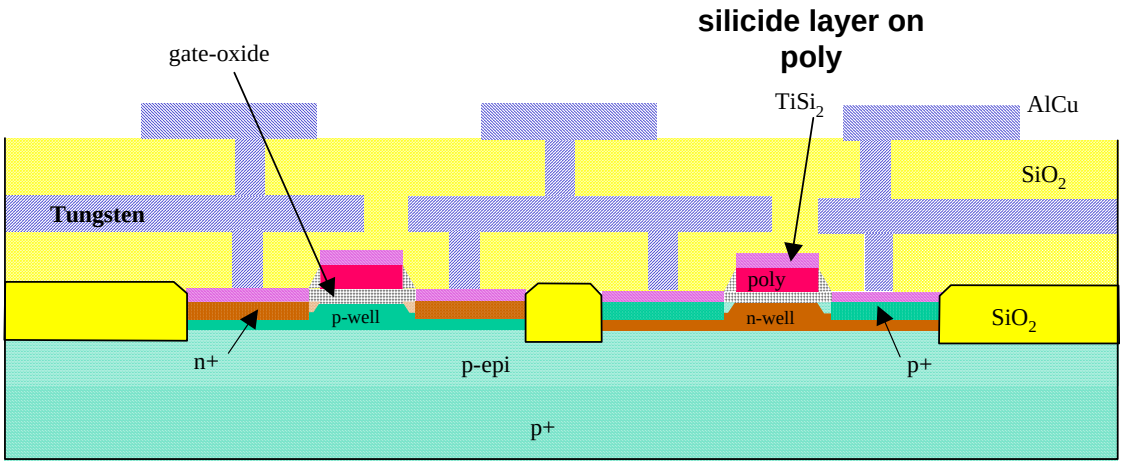


CMOS Process



Circa 1980s

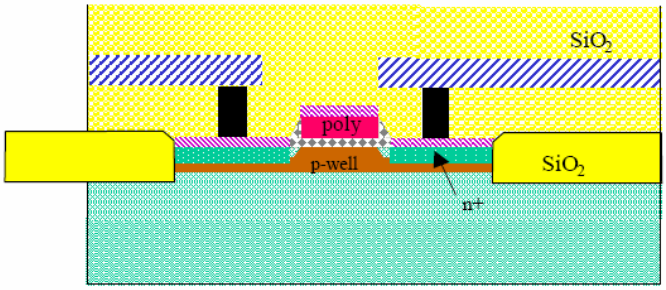
A Modern Dual-Well CMOS Process



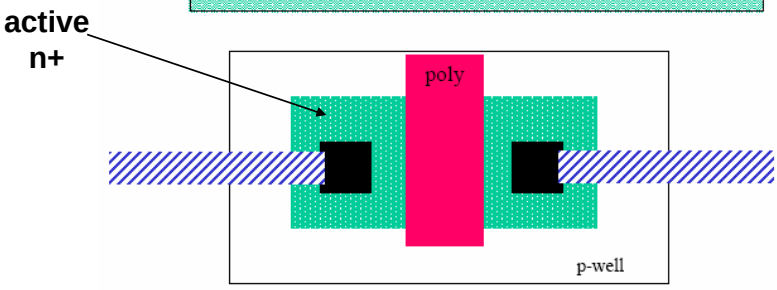
Dual-Well Trench-Isolated CMOS Process

Transistor Layout

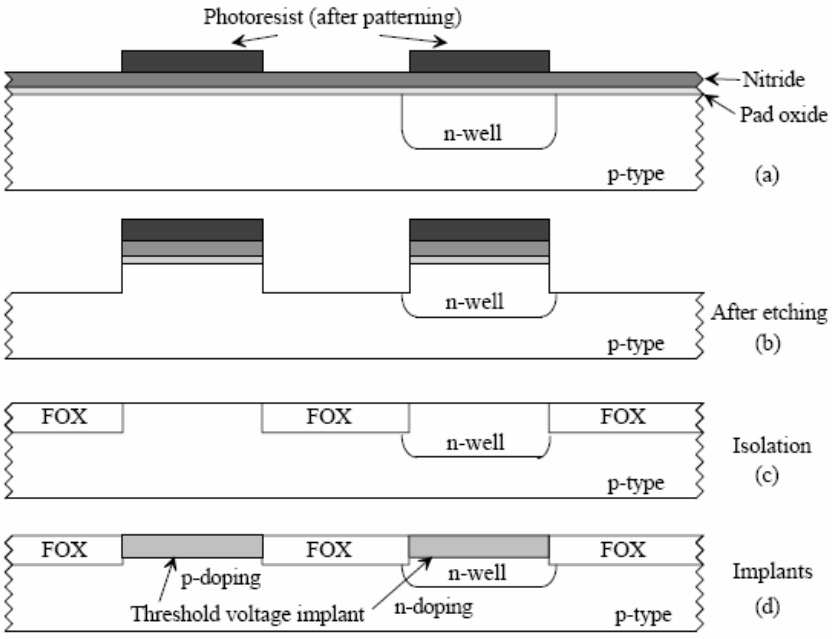
Cross-sectional view



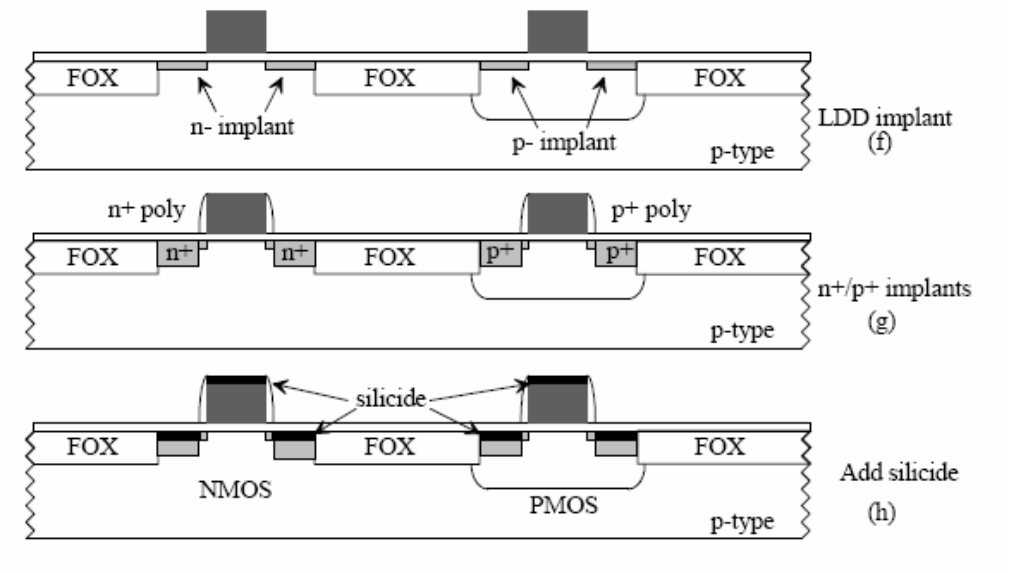
Layout view



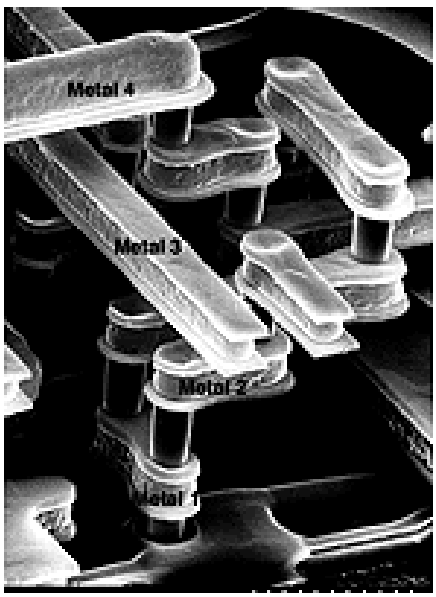
N-Well CMOS Flow



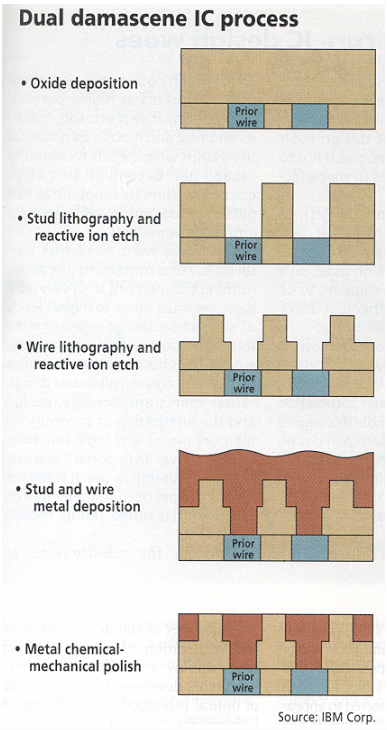
N-Well CMOS Flow

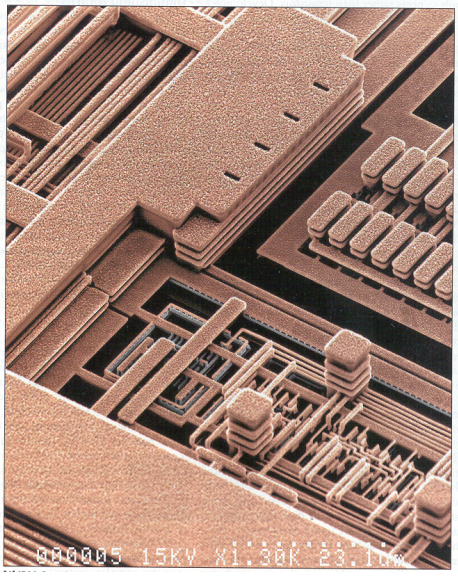


Advanced Metallization

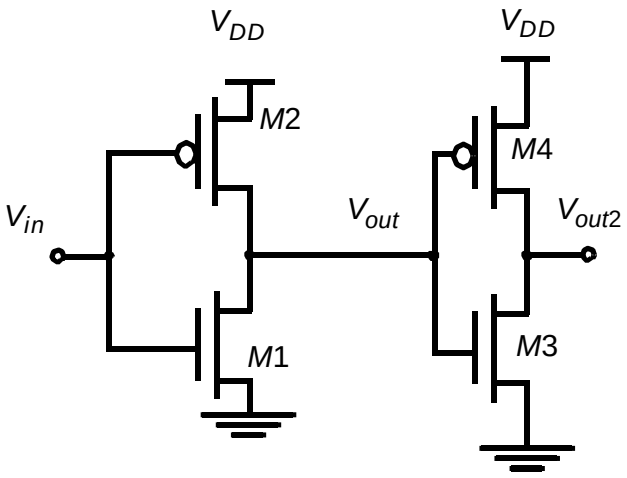


Advanced Metallization



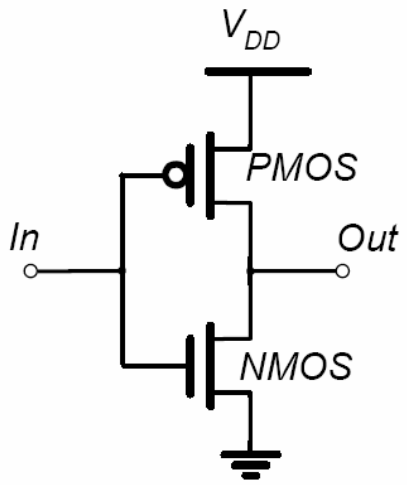


Circuit Under Design

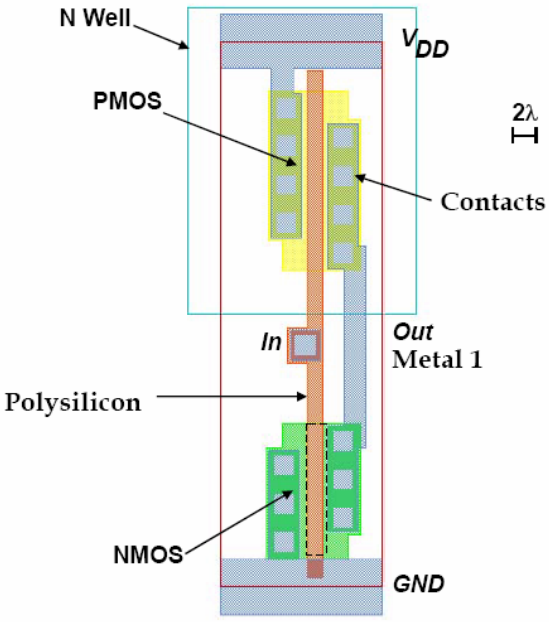


schematic

CMOS Inverter

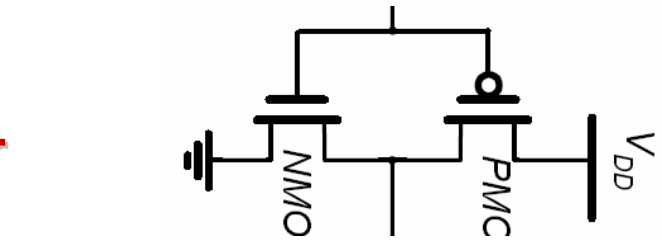


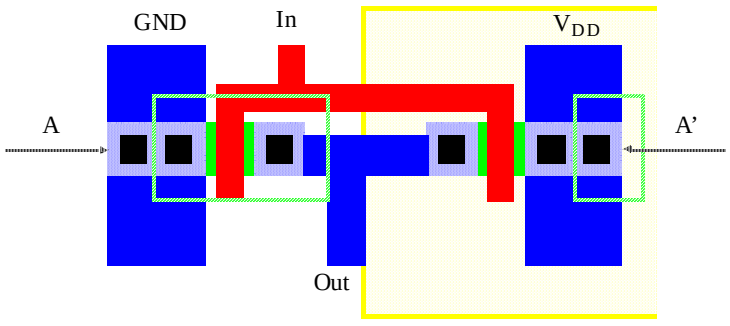
Schematic



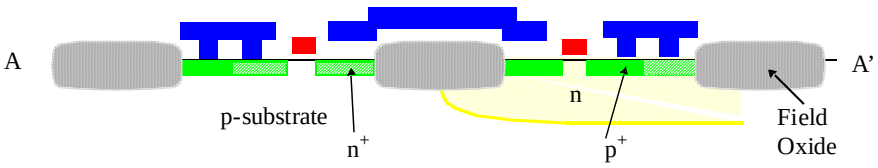
Layout

CMOS Inverter Layout



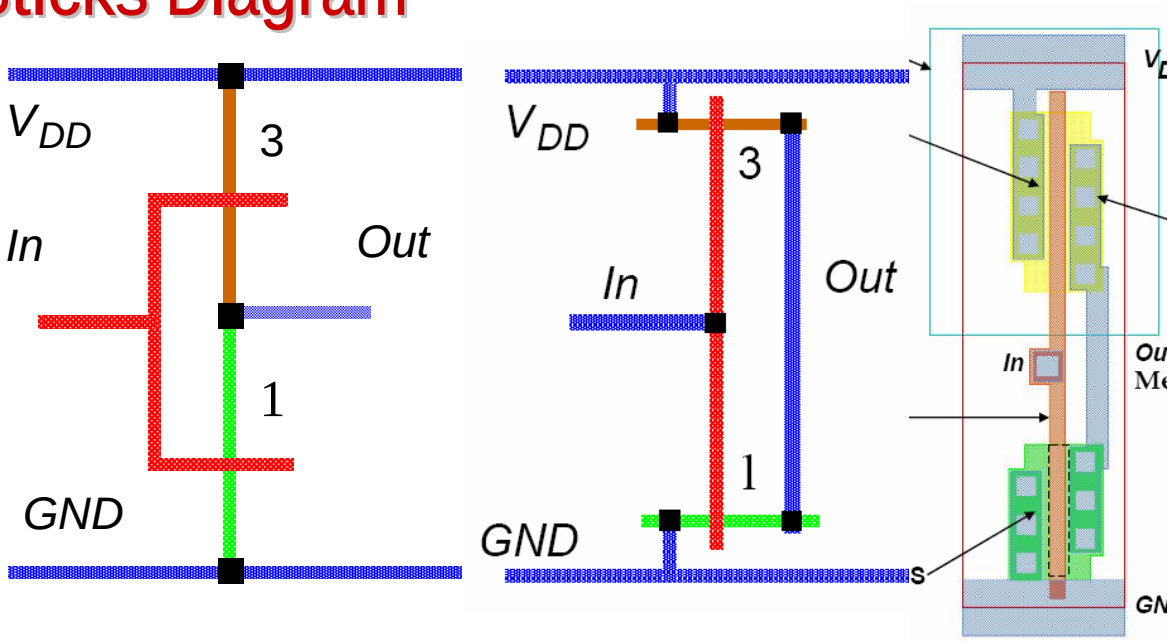


(a) Layout



(b) Cross-Section along A-A'

Sticks Diagram

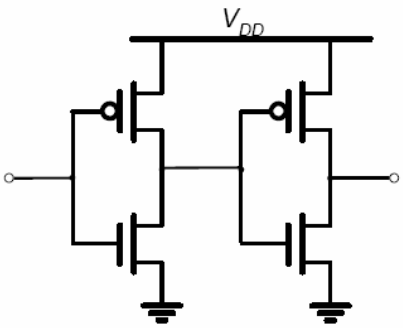


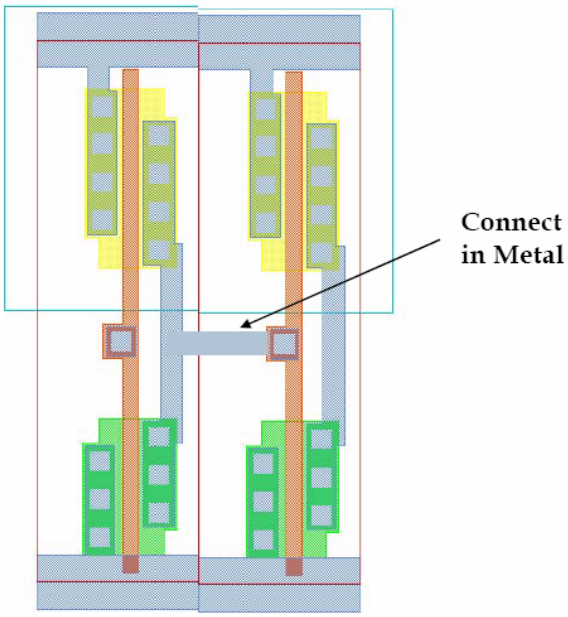
Stick diagrams of inverter

- Dimensionless layout entities
- Only topology is important

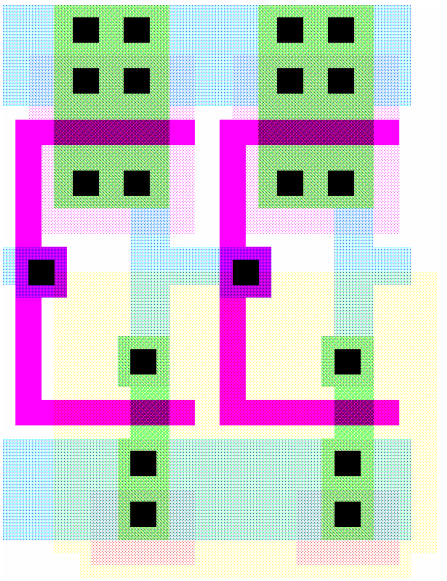
Two Inverters

- Share power and ground
- Abut cells





A Different Layout of Same 2 inverters



Design Rules

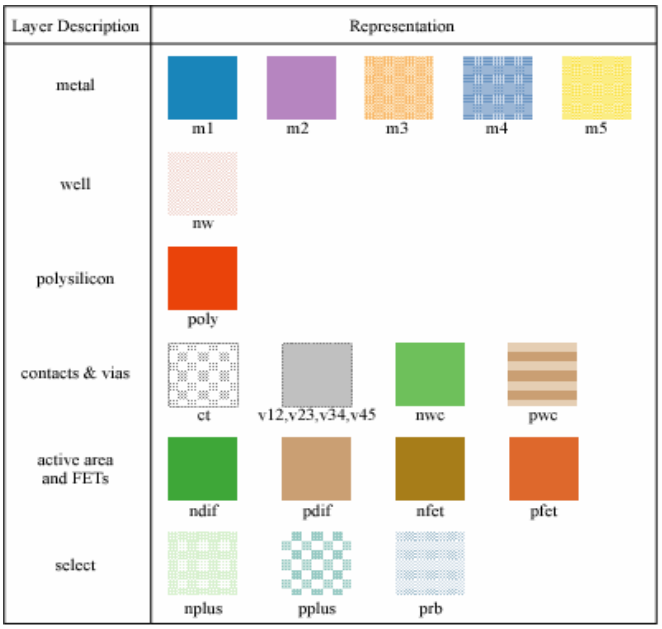
Design Rules

- **Interface between designer and process engineer**
- **Guidelines for constructing process masks**
- **Unit dimension: Minimum line width**
  - scalable design rules: lambda parameter
    - Less common now
  - absolute dimensions (micron rules)
    - More the standard now.

CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

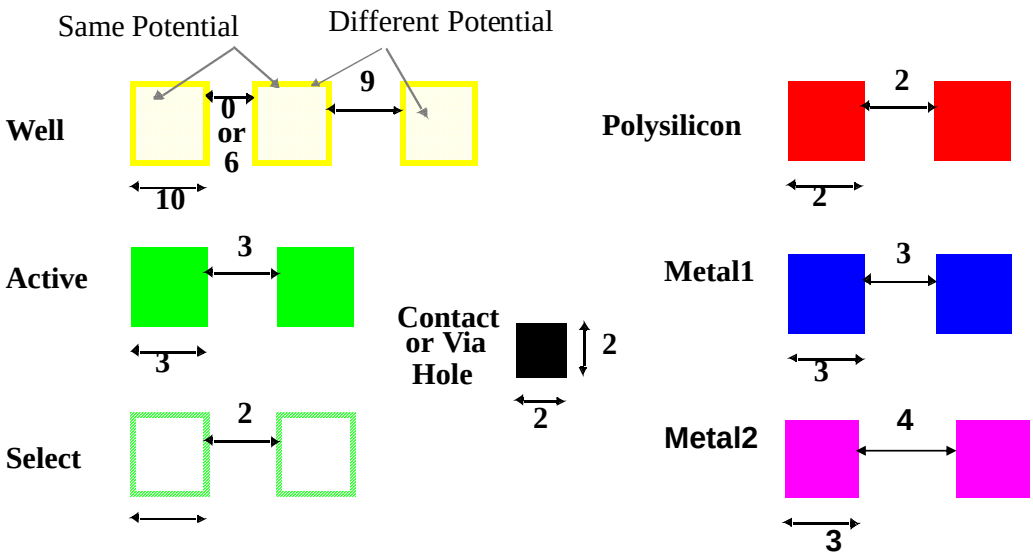
Layers in 0.25 μm CMOS process



Design Rules

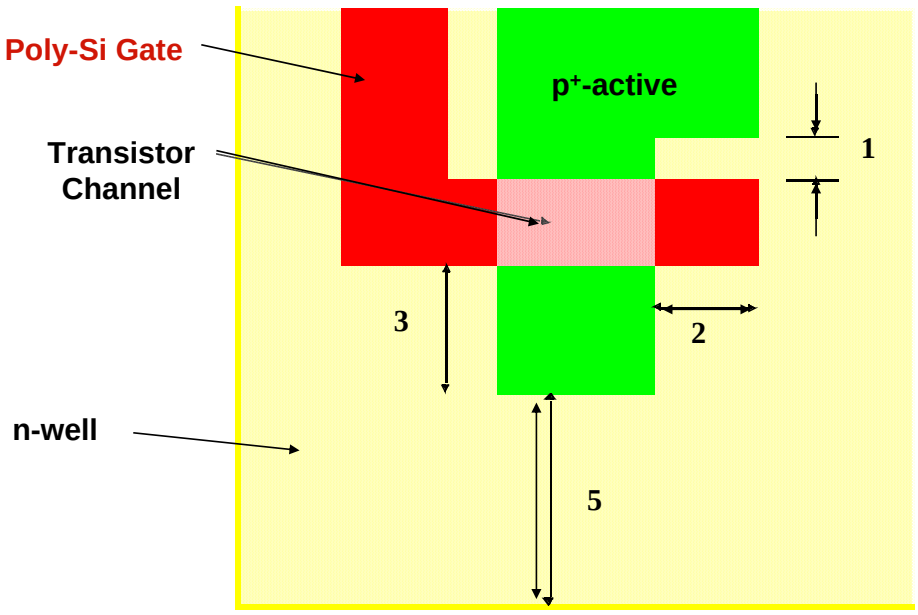
- **Intra-layer: widths, spacing**
- **Inter-layer: enclosures, overlaps**
  - Transistor rules
  - Contact and via rules
  - Well and substrate contacts
- **Special rules (sub-0.25 μm)**
  - Area, antenna rules, density rules

Intra-Layer Design Rules



Inter Layer: Transistor Layout

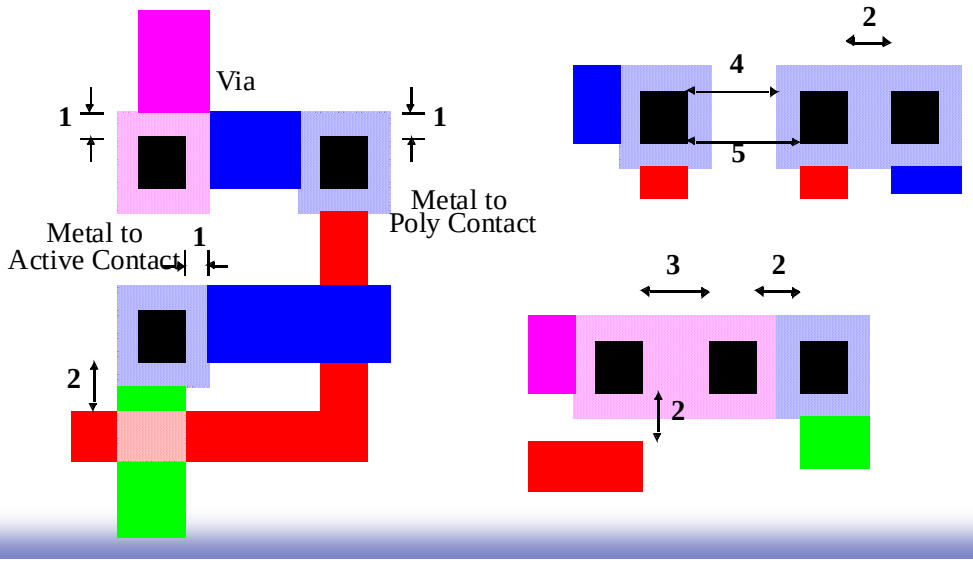
Self-aligned process



Is this an NMOS or PMOS transistor?

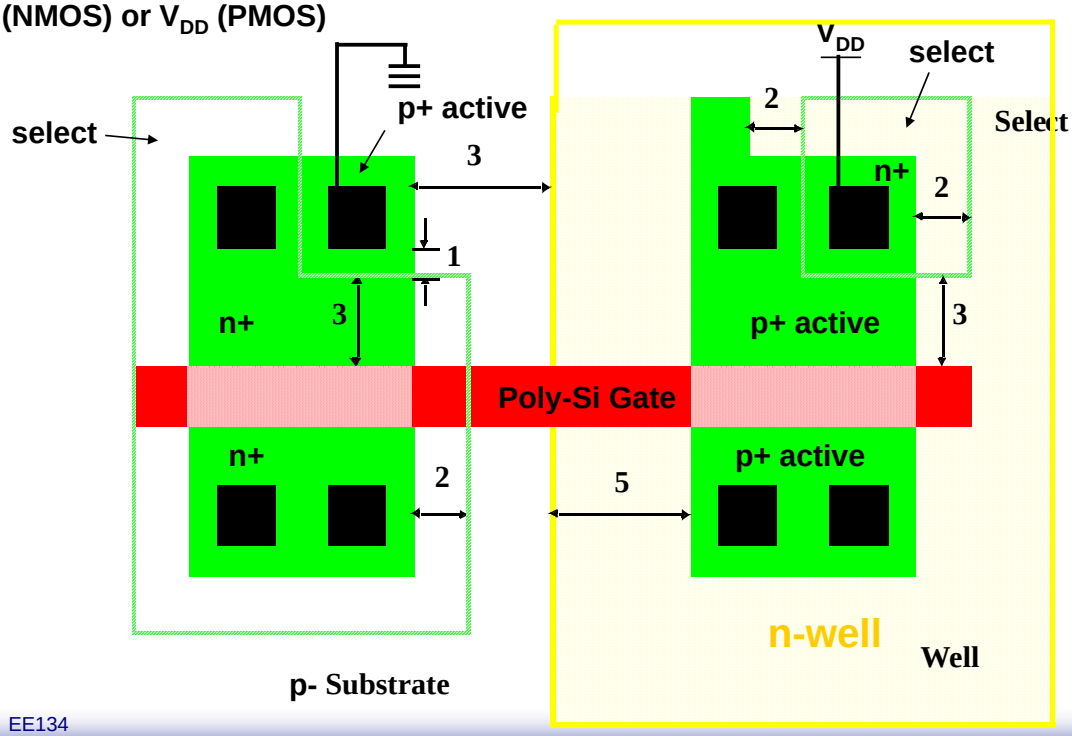
Inter Layer: Vias and Contacts

- Vias connect metal layer 1 (M1) to metal layer 2 (M2)
- Contacts connect M1 to the Si.
- Vias and contacts are always square (2x2 μm)
  - For large area contact, use many "contacts" in an array.



Select Layer

Select layer reverses the sign of the doping for pinning the substrate to ground (NMOS) or V_{DD} (PMOS)

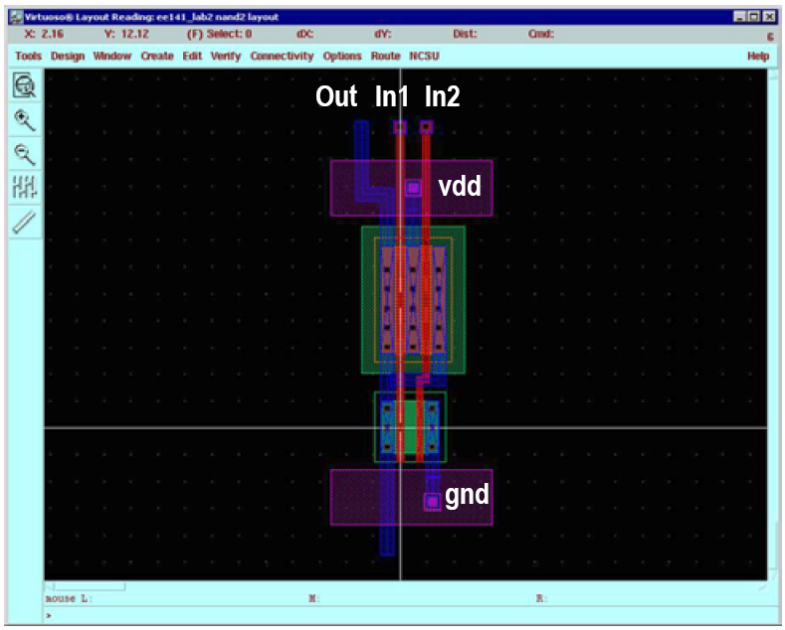


Actual Design Rule Example (MOSIS)

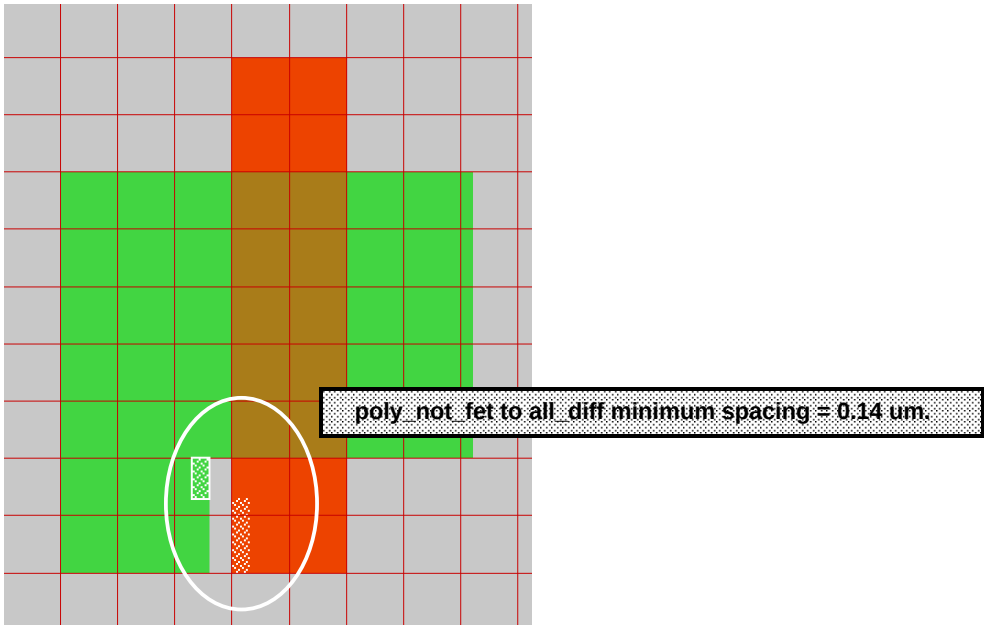
- http://www.mosis.org

http://www.mosis.org/Technical/Designrules/scmos/scmos-active.html

Cadence Layout Editor

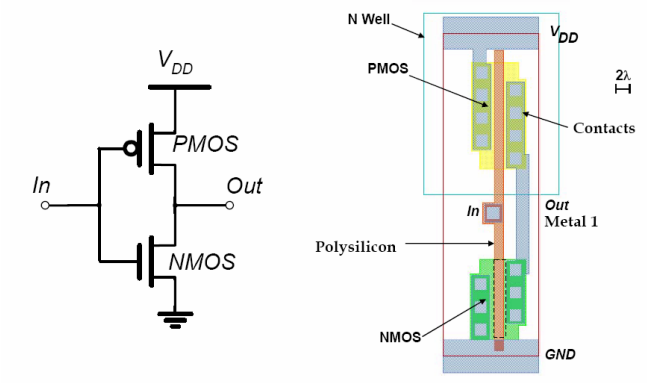


Design Rule Checker



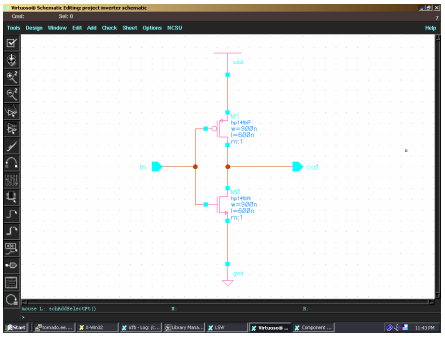
2 Types of Checks

- Design Rule Checking (DRC)
- Layout vs. Schematic (LVS)

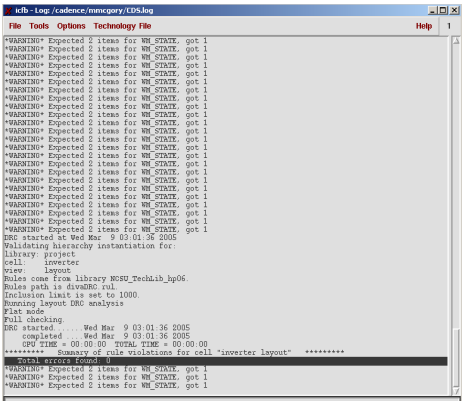


Schematic =? Layout

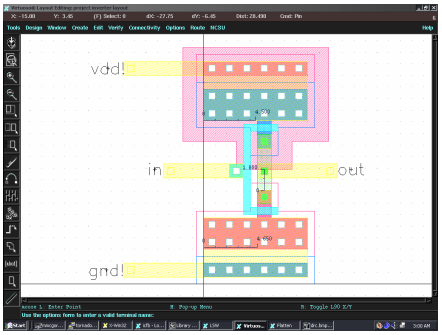
DRC and LVS



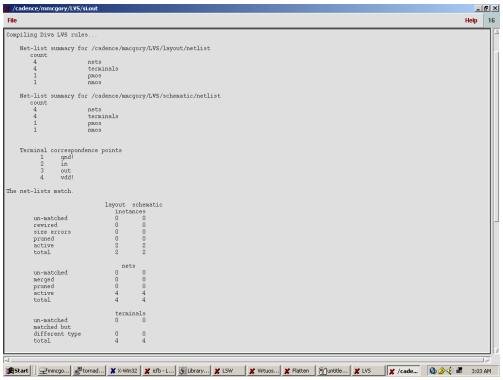
Schematic



Design Rule Check

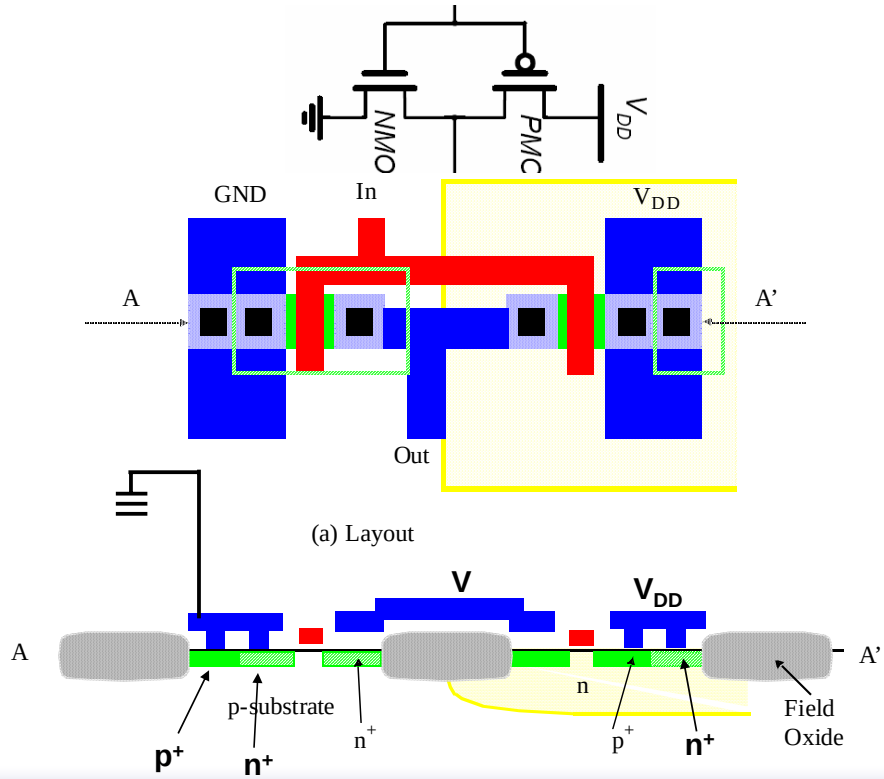


Layout



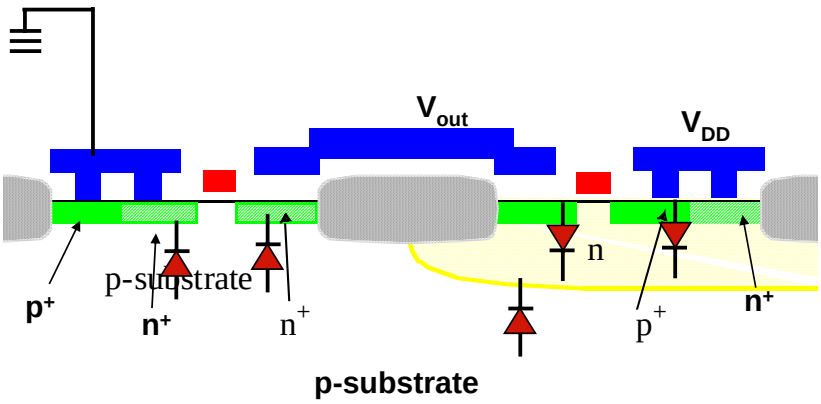
Layout vs. Schematic

Tie n-well to VDD and Substrate to Ground

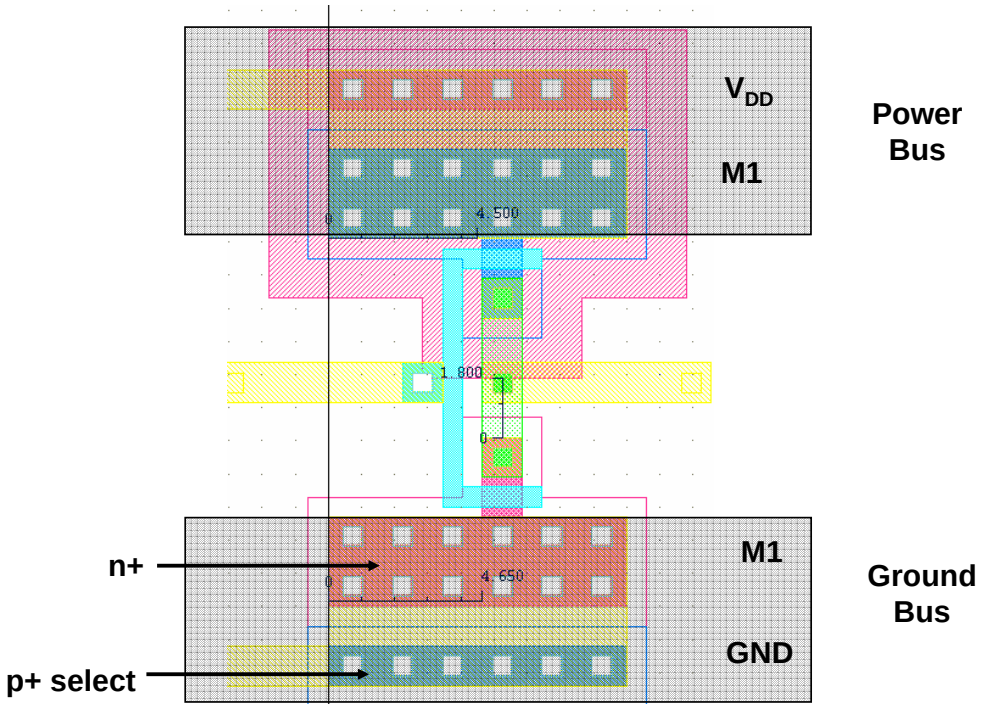


Reason for GND and V_{DD} Ties

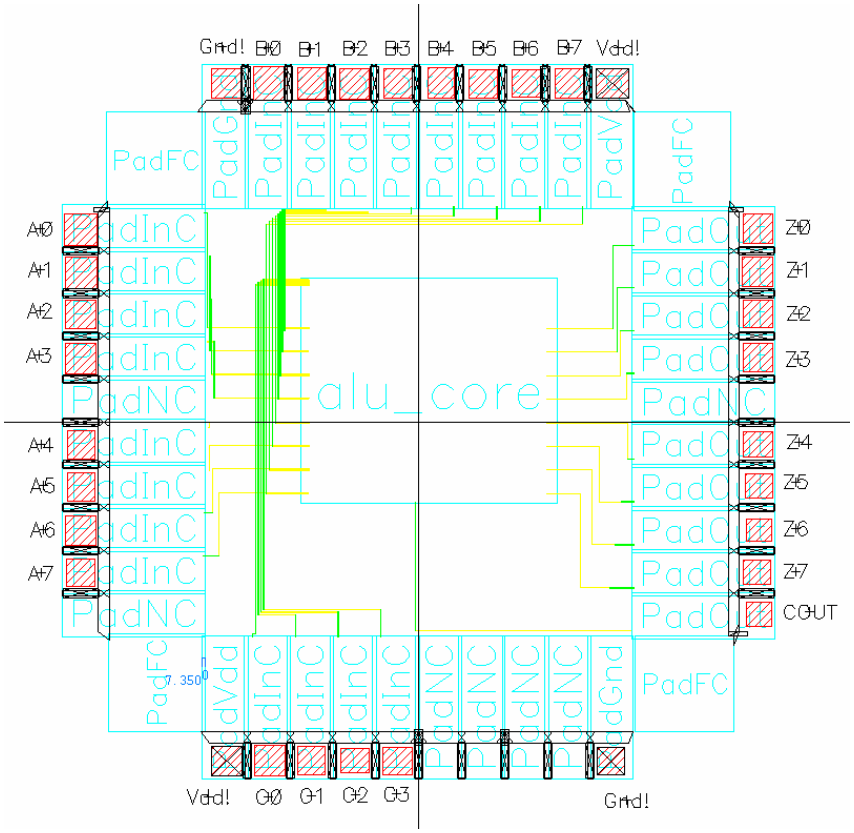
Parasitic Diodes



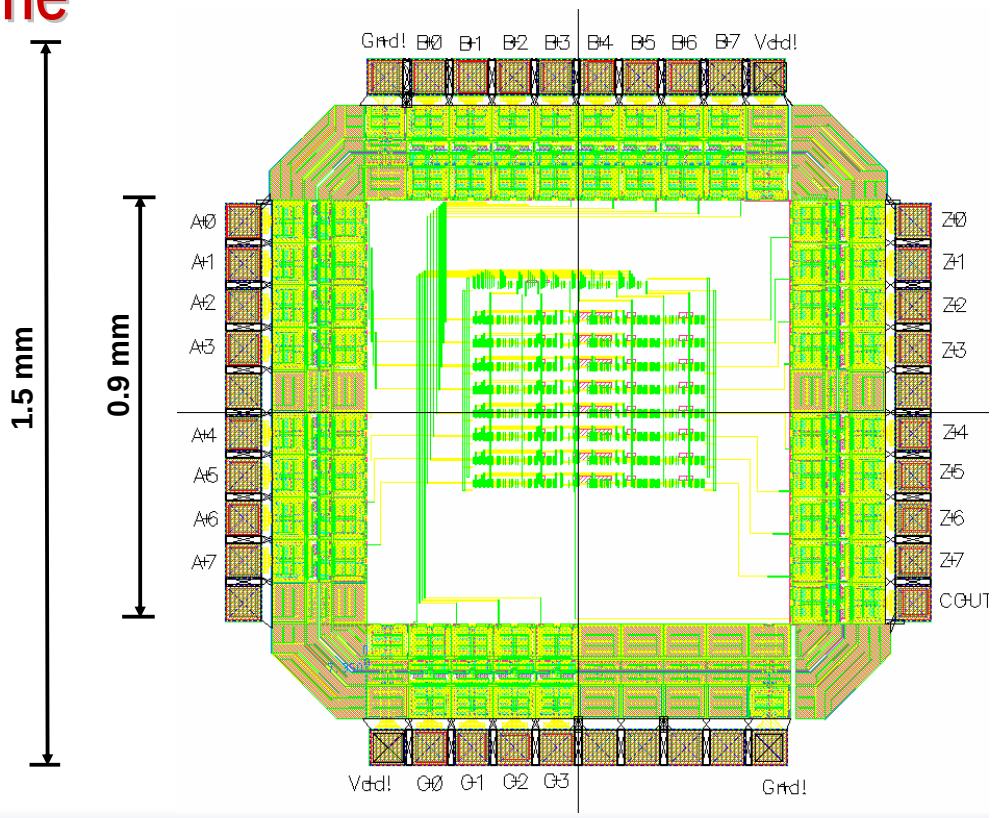
Pin n-well to V_{DD} and p-substrate to GND



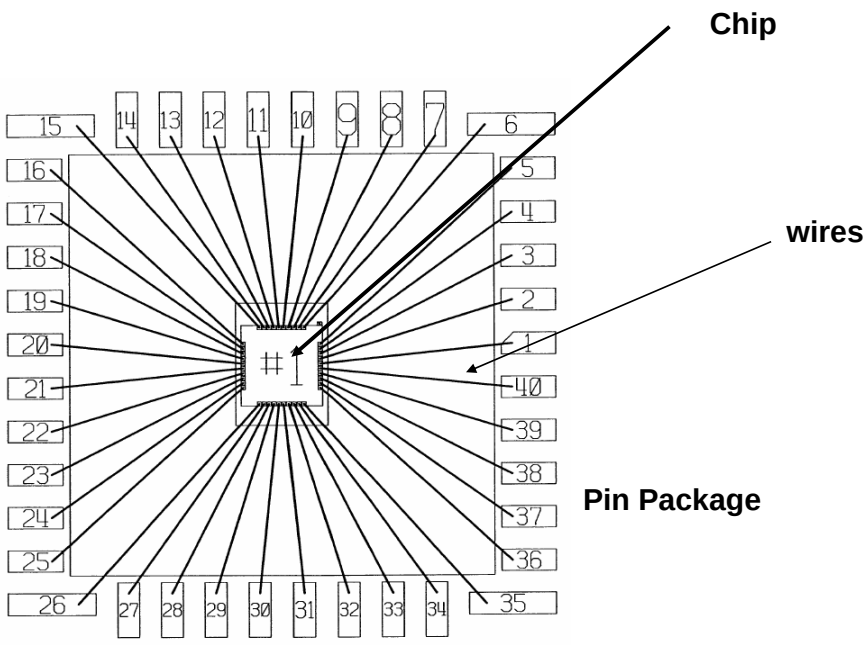
Padframe



Padframe



40 pin package



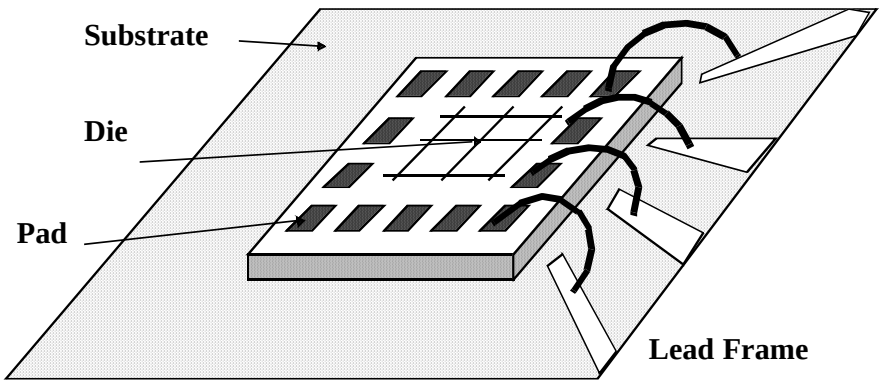
Packaging

Packaging Requirements

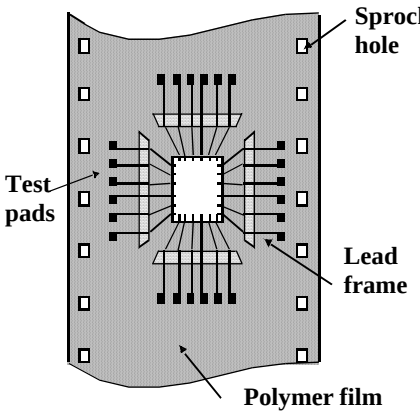
- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

Bonding Techniques

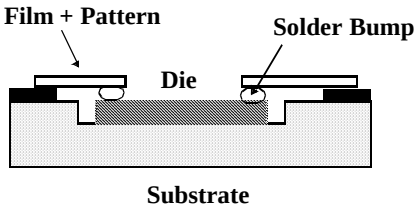
Wire Bonding



Tape-Automated Bonding (TAB)

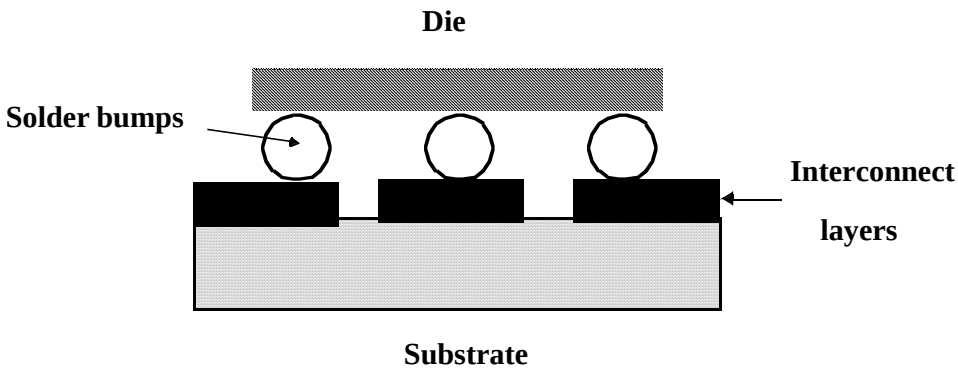


(a) Polymer Tape with imprinted wiring pattern.

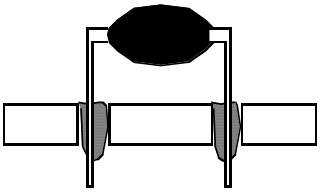


(b) Die attachment using solder bumps.

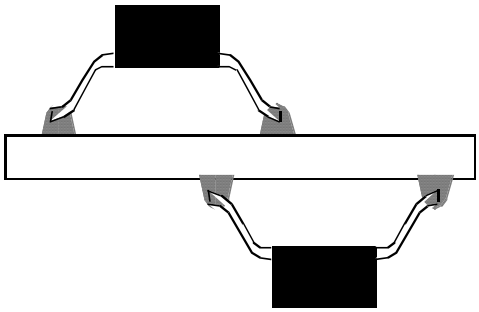
Flip-Chip Bonding



Package-to-Board Interconnect

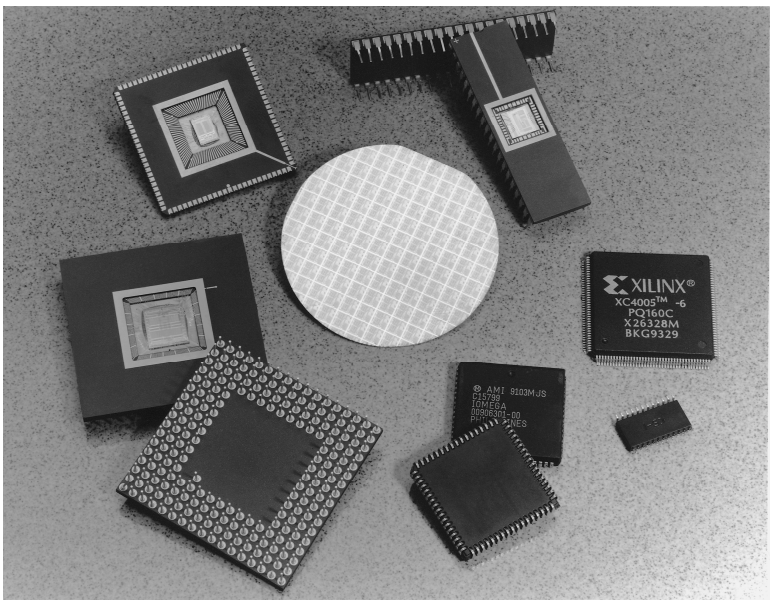


(a) Through-Hole Mounting



(b) Surface Mount

Package Types



Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Flowchart