Digital Integrated Circuit (IC) Layout and Design - Week 10, Lecture 20

- Midterm Due in Class
- Dynamic Logic
- SRAM
- Wrap up

Clocked CMOS Logic (C²MOS)

- Clocked CMOS Register (Positive Edge)

\( \phi_1 \) low:
- Master enabled. \( N1 = D \). M1 & M3 on.
- Slave latched. M6 and M7 off. Output Q is in charge storage mode (floating). Hi-Z state (high impedance).

\( \phi_1 \) high:
- Master Hi-Z state (\( N1 = \overline{D} \)).
- Slave enabled. \( Q_{n+1} = D_n \).

![Clocked CMOS Logic Diagram]
C\textsuperscript{2}MOS: Precharge – Evaluate (PE) Logic

**General Concept**

CLK = 0: Precharge output Z = V\textsubscript{dd}. 
M\textsubscript{e} off; M\textsubscript{p} on. Z = V\textsubscript{dd}.

CLK = 1: Evaluate. M\textsubscript{e} off. M\textsubscript{p} on. 
Pull down Z (or not) depending on logic implemented in PDN.

**Specific Example**

CLK = 0: Precharge Z = 1
CLK = 1: Evaluate. Z = (AB + C)

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Domino Logic

- Like falling dominoes.

CLK=0: Precharge
CLK=1: Logic propagates thru series of gates like dominoes falling.
Domino Logic with Keeper at output

- Use small $M_{kp}$

Dynamic Shift Register

- Non-overlapping clock
Non-Overlapping CLK

Initially, CLK=1 (Black). \( \phi_1 = 1 \) & \( \phi_2 = 0 \).

CLK \( \Rightarrow \) 0 (Red)
CLK \( \Rightarrow \) 1 (Blue)

Static RAM (SRAM)

- SRAM Cell: Simple D-FF (Latch)
  - Word line low:
    - Pass transistors M5 and M6 off.
    - Data latched in inverter pair.
  - Word line high: Writing / Reading
    - Writing: Write by force.
    - Reading: BIT and BIT precharged to either V_{DD} or V_{DD}/2. Read.
SRAM at transistor level

EE134 Summary

- Major Challenges
  - Cost
  - Power Consumption
  - Robustness
  - Complexity

- Some new circuit solutions and design methodologies are coming.
### Technology Scaling

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology Node (nm)</th>
<th>Integration Capacity (GT)</th>
<th>Delay Scaling</th>
<th>Energy Scaling</th>
<th>Bulk Planar CMOS</th>
<th>Alternative 30 nm</th>
<th>Variability</th>
<th>C/D (V)</th>
<th>RC Delay</th>
<th>Metal Layers</th>
<th>Oxide</th>
<th>SiGe S/D PMOS</th>
<th>1.2nm Ultra-thin SiO2</th>
<th>High-K &amp; Metal-Gate Options</th>
<th>Non-planar Tri-Gate Architecture Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>11</td>
<td>8</td>
<td>0.7</td>
<td>&gt;0.5</td>
<td>High Probability</td>
<td>Low Probability</td>
<td>Medium</td>
<td>&gt;3</td>
<td>1</td>
<td>0.7</td>
<td>~3</td>
<td>~3</td>
<td>~3</td>
<td>High-K &amp; Metal-Gate Options</td>
<td>Non-planar Tri-Gate Architecture Option</td>
</tr>
<tr>
<td>2017</td>
<td>8</td>
<td>4</td>
<td>&gt;0.7</td>
<td>&gt;0.5</td>
<td>Low Probability</td>
<td>High Probability</td>
<td>High</td>
<td>1.1</td>
<td>1</td>
<td>7.8</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>High-K &amp; Metal-Gate Options</td>
<td>Non-planar Tri-Gate Architecture Option</td>
</tr>
<tr>
<td>2016</td>
<td>6</td>
<td>4</td>
<td>1</td>
<td>0.5</td>
<td>Low Probability</td>
<td>High Probability</td>
<td>Very High</td>
<td>1</td>
<td>1</td>
<td>8.0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>High-K &amp; Metal-Gate Options</td>
<td>Non-planar Tri-Gate Architecture Option</td>
</tr>
</tbody>
</table>

### Research Roadmap

- **2015-2019 Research**
  - **65nm Node 2005**
  - **32nm Node 2009**
  - **22nm Node 2011**
  - **10nm Length (Research)**
  - **Enanotube Prototype (Research)**
  - **Nanowire Prototype (Research)**
  - **III-V Device Prototype (Research)**
  - **High-K & Metal-Gate Options**
  - **Non-planar Tri-Gate Architecture Option**

Robert Chau, Intel, ICSICT 2004
Device Evolution

Conventional Processing (being done in 300nm fabs)

- Top-down Approach
  - std litho and etch
  - Integration with Si?

Bottom-up Approach
- Chirality issues
- Positioning issues
  (required > 10 billion gates)

Robert Chau, Intel, ICSICT 2004

25 nm FinFET

25 nm MOS transistor (Folded Channel)
Cost

- Mask cost in 90nm technology is over $1M.
- Bugs are very expensive.
- Design effort increases in DSM.
- Cost of new tools.
- Non-recurring costs dominate the price effectiveness of low-volume ASICs.
- Need to have a product that can fit multiple applications, customers (flexibility).

Power has become a Problem

![Power Graph]

Power delivery and dissipation will be prohibitive

Source: S. Borkar (Intel)
The Productivity Gap

Challenges in Digital Design

- The Deep Submicron (DSM) Effect
  - ∝ DSM
    - “Microscopic Problems”
      - Ultra-high speed design
      - Interconnect
      - Noise, Crosstalk
      - Reliability, Manufacturability
      - Power Dissipation
      - Clock distribution.
    - Everything Looks a Little Different
  - ∝ 1/DSM
    - “Macroscopic Issues”
      - Time-to-Market
      - Millions of Gates
      - High-Level Abstractions
      - Reuse & IP: Portability
      - Predictability
      - etc.
    - ...and There’s a Lot of Them!
ABET Evaluation: Course Objectives

Things that you should have learned in EE134.

<table>
<thead>
<tr>
<th>Course Objective</th>
<th>Very Poorly</th>
<th>Very Well</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Understand the device model for a modern short-channel FET.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>2 Understand the parasitic diodes and capacitors of an inverter.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>3 Ability to layout, DRC, and LVS a CMOS digital IC.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>4 Calculate delay times through inverters and logic gates.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>5 Size a chain of inverters to drive a large capacitive load.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>6 Design static CMOS logic gates.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>7 Understand CMOS transmission gates.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>8 Understand CMOS transmission gate latches and registers.</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
</tbody>
</table>

ABET: Program Outcomes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Very Poorly</th>
<th>Very Well</th>
</tr>
</thead>
<tbody>
<tr>
<td>a An ability to apply knowledge of mathematics, science, and engineering</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>b An ability to design and conduct experiments, as well as to analyze and interpret data</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>c An ability to design a system, component, or process to meet desired needs</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>d An ability to function on multi-disciplinary teams</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>e An ability to identify, formulate, and solve engineering problems</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>f An understanding of professional ethical responsibility</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>g An ability to communicate effectively</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>h The broad education necessary to understand the impact of engineering solutions in a global and societal context</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>i A recognition of the need for, and an ability to engage in life-long learning</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>j A knowledge of contemporary issues</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
<tr>
<td>k An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice</td>
<td>1 2 3 4 5</td>
<td></td>
</tr>
</tbody>
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