Digital Integrated Circuit (IC) Layout and Design

EE 134 – Winter 05

- Lecture Tu & Thurs. 9:40 – 11am ENGR2 142
- 2 Lab sections
  - M 2:10pm – 5pm ENGR2 128
  - F 11:10am – 2pm ENGR2 128

- NO LAB THIS WEEK
- FIRST LAB Friday Jan. 20

People

- Lecturer - Roger Lake
  - Office – ENGR2 Rm. 437
  - Office hours - MW 4-5pm
  - rlake@ee.ucr.edu

- TA – Faruk Yilmaz
  - Office – ENGR2 Rm. 222
  - Office Hours – TBD
  - faruk@ee.ucr.edu
EE134 Web-site

- [http://www.ee.ucr.edu/~rlake/EE134.html](http://www.ee.ucr.edu/~rlake/EE134.html)
  - Class lecture notes
  - Assignments and solutions
  - Lab and project information
  - Exams and solutions
  - Other useful links

Text Book

**Digital Integrated Circuits: A Design Perspective, 2nd Ed.**

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic
Homework Week 1

- Read Chapter 1 of text.

Last Lecture

- Last lecture
  - Moore’s Law
  - Challenges in digital IC design for next decade
- Today
  - Review of Moore’s Law
  - Design metrics
Summarizes progress in complexity of ICs

1971

2,300 transistors
108 KHz operation
Hand Crafted

P4 2000

42 M transistors
1.5 GHz operation
Standard Cell
Automated Design
VLSI

~ 15,000 x

Moore’s Law

* In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

* He made a prediction that semiconductor technology will double its effectiveness every 18 months
Moore’s Law

Log of the number of components per integrated function

Electronics, April 19, 1965.

Evolution in Complexity

Number of bits per chip

Human memory
Human DNA

4 Gbits
0.15-0.2µm

256 Mbits
0.25-0.3µm

64 Mbits
0.35-0.4µm

16 Mbits
0.5-0.6µm

4 Mbits
0.7-0.8µm

1 Mbit
1.0-1.2µm

256 Kbits
1.6-2.4µm

64 Kbits
Page

Encyclopedia
2 hrs CD Audio
30 sec HDTV

Year
Transistor Counts

Moore’s law in Microprocessors

Transistors on Lead Microprocessors double every 2 years
Die Size Growth

Die size grows by 14% / 2 yrs. to satisfy Moore’s Law

Frequency

Lead Microprocessors frequency doubles every 2 years
Transistors on Lead Microprocessors double every 2 years
Die size grows by 14% / 2 yrs.
Power will be a major problem

Power delivery and dissipation will be prohibitive

Productivity Trends

• Electronic design automation (EDA) tools to deal with complexity.
  • Cadence
Why Scaling?

- Technology shrinks by 0.7/generation
  - # of transistors / die doubles every 2 years.
  - Can integrate 2x more functions per chip.
  - Cost per function decreases by 2x.
- Main problem: power delivery and dissipation.

How to design more and more complex chips?

- Designer productivity does not double every two years.
- Understand and exploit different levels of abstraction.
- Automated tools (EDA).

Design Abstraction Levels

Started with large scale – microprocessors.

Go down to gate level, transistor level, then back up.
2010 Outlook

- **Performance 2x / 2 years**
  - 1 T (Tera) instructions / s
  - 20 – 30 GHz clock

- **Complexity**
  - # transistors: 1 Billion
  - Die area: 40mm x 40mm

- **Power**
  - 10 kW!
  - Leakage: 1/3 of total power

Design Metrics

- **How to evaluate performance of a digital circuit (gate, block, ...)?**

- **Outline**
  - **Cost**
  - Reliability
  - Speed
  - Power
Cost of Integrated Circuits

- **NRE (Non-Recurrent Engineering) costs - fixed**
  - Design time and effort, mask generation
    - Independent of sales volume / number of products
    - One-time cost factor
  - Indirect costs (company overhead)
    - R&D, manufacturing equipment (Fab), etc.

- **Recurrent costs - variable**
  - silicon processing, packaging, test
    - proportional to **volume**
    - proportional to **chip area**

NRE Cost is Increasing

“...the club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive.”

Ron Wilson, EE Times (May 2000)

70nm ASICs will have $4M NRE
Total Cost

- **Cost per IC**
  
  \[
  \text{Cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}
  \]

- **Variable cost**

  \[
  \text{Variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}
  \]

---

Die Cost

- **Wafer**

- **Single die**

  \[
  \text{cost of die} = \frac{\text{cost of wafer}}{\text{Dies per wafer} \times \text{die yield}}
  \]

From [http://www.amd.com](http://www.amd.com)

Going up to 12” (30cm)

8 – 12”
**Yield**

\[ Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

Die cost = \( \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \)

Dies per wafer = \( \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}} \)

**Defects**

\[ \text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha} \]

\( \alpha \approx 3, \text{ complexity of mfg. process} \)

Defects per unit area = 0.5 – 1 / cm²

\[ \text{die cost} = f \left(\text{die area}\right)^4 \]
die cost = \( f (\text{die area})^4 \)

\[
\text{die cost} = \frac{\text{Wafer cost}}{\text{dies per wafer} \times \text{Die yield}}
\]

\[
dies \text{ per wafer} \propto \frac{1}{\text{die area}}
\]

\[
\text{die yield} = \left( 1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}
\]

\[
\alpha = 3
\]

\[
die \text{ yield} \propto \left( \frac{1}{\text{die area}} \right)^3
\]

\[
die \text{ cost} \propto (\text{die area})^4
\]

---

### Some Examples (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Cost per Transistor

Fabrication capital cost per transistor (Moore’s law)

Today:
~10,000 transistors / penny
~100 n$/transistor

Outline

- Design Metrics
  - Cost
  - Reliability - Noise
  - Speed
  - Power
Reliability — Noise in Digital Integrated Circuits

signal lines

\[ i(t) \]

Inductive coupling

\[ v(t) \]

Capacitive coupling

Power and ground noise

- Noise sources
  - Internal (proportional to signal swing)
  - External (not related to signal levels)

DC Operation

**Voltage Transfer Characteristic**

\[
\begin{align*}
V_{\text{OH}} & = V_{\text{Out High}} \\
V_{\text{OL}} & = V_{\text{Out Low}} \\
V_{\text{M}} & = \text{Switching threshold} \\
V_{\text{SW}} & = \text{Signal swing} = V_{\text{OH}} - V_{\text{OL}}
\end{align*}
\]

How much can input signal deviate from \( V_{\text{OH}} \) and \( V_{\text{OL}} \) and circuit still work?
Mapping between analog and digital signals

“1”

V_{OH} \hspace{1cm} V_{IH}

Undefined Region

“0”

V_{IL} \hspace{1cm} V_{OL}

V_{IL} is maximum voltage at input that is a “0”.
V_{IH} is minimum voltage at input that is a “1”.
In between is undefined.

Definition of Noise Margins

Gate Output (Stage M) \hspace{5cm} Gate Input (Stage M+1)

Noise margin high

N_{MH} = V_{OH} - V_{IH}

Noise margin low

N_{ML} = V_{IL} - V_{OL}
Noise Budget

Allocate gross noise margin to expected sources of noise

Sources:
- power supply (noise on power supply / ground)
- offset
- cross talk (inductive and capacitance)
- Interference (consecutive signals)
- Timing (jitter and skew)

Differentiate between fixed and proportional noise sources

Key Reliability Properties

Absolute noise margin values are deceptive
- a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

Noise immunity is the more important metric – the capability to suppress noise sources

Key metrics:
- Noise transfer functions
- Output impedance of the driver
- Input impedance of the receiver
Regenerative Property

A chain of inverters

Simulated response
**Fan-in and Fan-out**

Fan-out $N$

Fan-in $M$

**The Ideal Gate**

$R_i = \infty$

$R_o = 0$

Fanout $= \infty$

$NM_H = NM_L = V_{DD}/2$
An Old-time Inverter

Outline

- Design Metrics
  - Cost
  - Reliability - Noise
  - Speed
  - Power
Delay Definitions

Defined w.r.t. output

\[ V_{in} \]
\[ V_{out} \]

\[ t_p = \frac{t_{pLH} + t_{pHL}}{2} \]

Lot of output loading \( C_L \) increase \( t_r \) and \( t_f \)

\[ t_{pHL} - \text{output high to low delay time} \]
\[ t_{pLH} - \text{output low to high delay time} \]
\[ t_p - \text{propagation delay} \]
\[ t_r - \text{rise time} \]
\[ t_f - \text{fall time} \]

\( t_p \) is an mostly used to compare different technologies. Artificial metric.
Ring Oscillator – measuring $t_p$

$T = 2 \times t_p \times N$

A First-Order RC Network

$v_{out}(t) = (1 - e^{-t/\tau}) V_{in}$

$t_p = \ln (2) \tau = 0.69 \text{ RC}$

Delay: 0.69 RC
90% point: 2.2 RC

Important model – matches delay of inverter
Power Dissipation

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}} i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}} i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t) dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t) dt \]

Energy and Energy-Delay

Power-Delay Product (PDP) =
\[ E = \text{Energy per operation} = P_{av} \times t_p \]

Energy-Delay Product (EDP) =
\[ \text{quality metric of gate} = E \times t_p \]
A First-Order RC Network

\[ \begin{align*}
E_{0 \to 1} &= T \int_0^T P(t) dt = V_{dd} \int_0^T i_{\text{supply}}(t) dt = V_{dd} \int_0^T C_L dV_{out} = C_L \cdot V_{dd}^2 \\
E_{\text{cap}} &= T \int_0^T P_{\text{cap}}(t) dt = V_{dd} \int_0^T V_{out}^2 dt = \frac{1}{2} C_L \cdot V_{dd}^2
\end{align*} \]

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Get a clear perspective on the challenges and potential solutions
- Understand the design metrics that govern digital design
  - Cost, reliability, speed, power and energy dissipation