Digital Integrated Circuit (IC) Layout and Design

❑ EE 134 – Winter 05

- Lecture Tu & Thurs. 9:40 – 11am ENGR2 142
- 2 Lab sections
  - M 2:10pm – 5pm ENGR2 128
  - F 11:10am – 2pm ENGR2 128
- NO LAB THIS WEEK
- FIRST LAB Friday Jan. 20

People

❑ Lecturer - Roger Lake

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- Office hours - MW 4-5pm
- rlake@ee.ucr.edu

❑ TA – Faruk Yilmaz

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- Office Hours – TBD
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EE134 Web-site

- http://www.ee.ucr.edu/~rlake/EE134.html
  - Class lecture notes
  - Assignments and solutions
  - Lab and project information
  - Exams and solutions
  - Other useful links

Text Book

Digital Integrated Circuits:
A Design Perspective, 2nd Ed.

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Homework Week 1

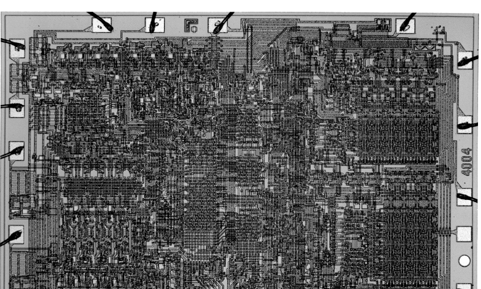
- Read Chapter 1 of text.

Last Lecture

- Last lecture
  - Moore's Law
  - Challenges in digital IC design for next decade
- Today
  - Review of Moore's Law
  - Design metrics

Summarizes progress in complexity of ICs

1971

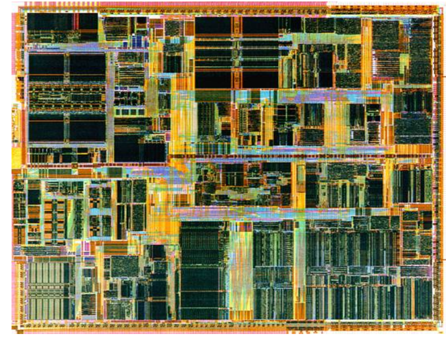


2,300 transistors
108 KHz operation

Hand Crafted

~ 15,000 x

P4 2000



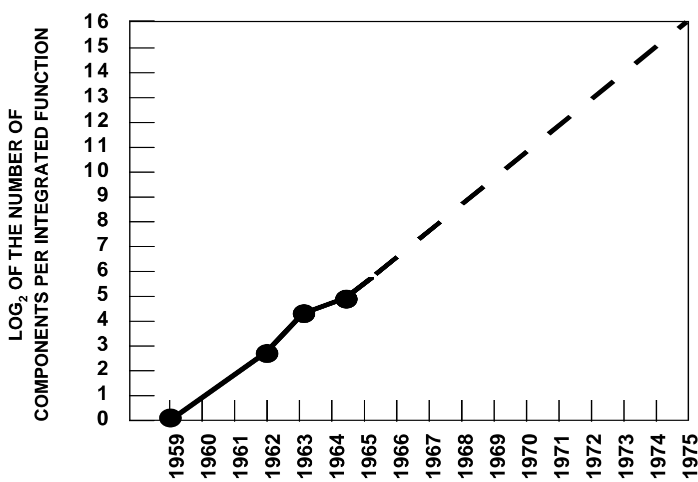
42 M transistors
1.5 GHz operation

Standard Cell
Automated Design
VLSI

Moore's Law

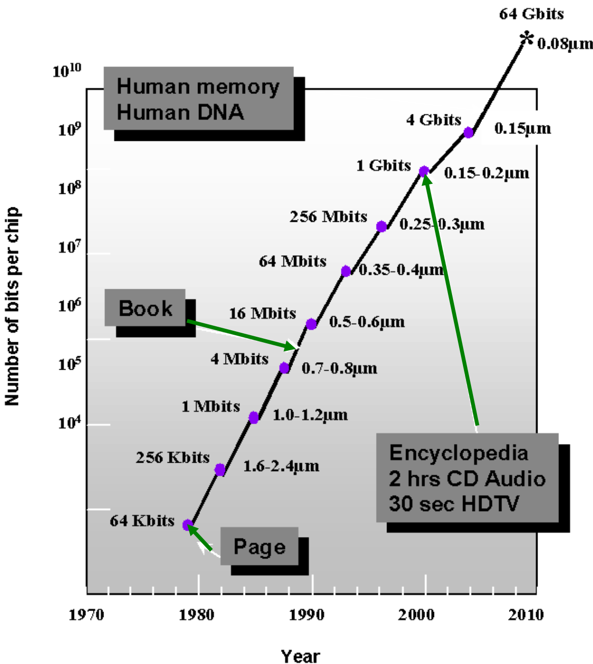
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

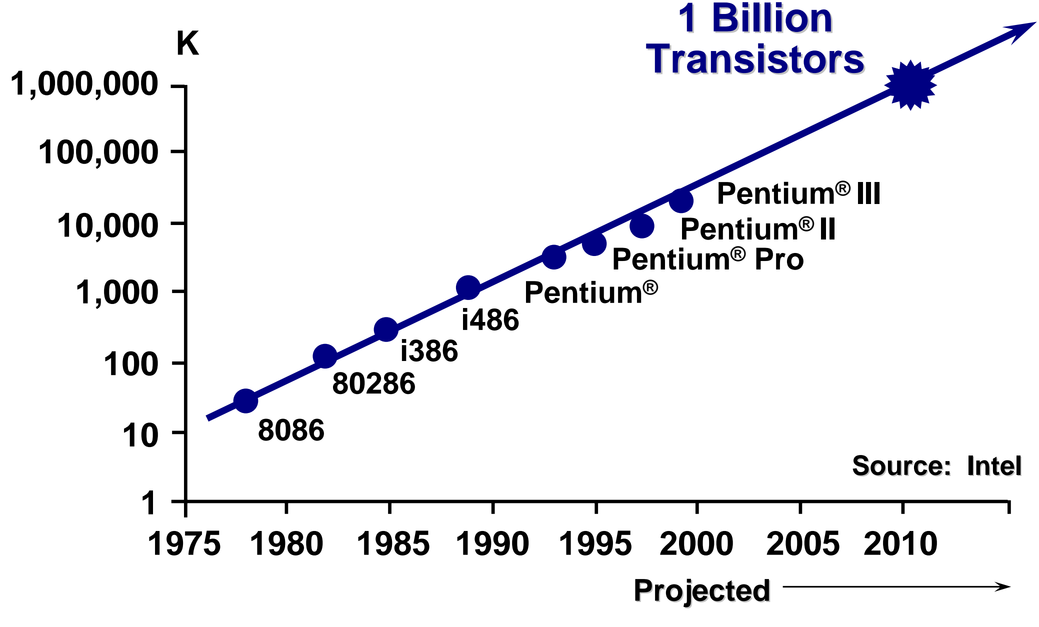


Electronics, April 19, 1965.

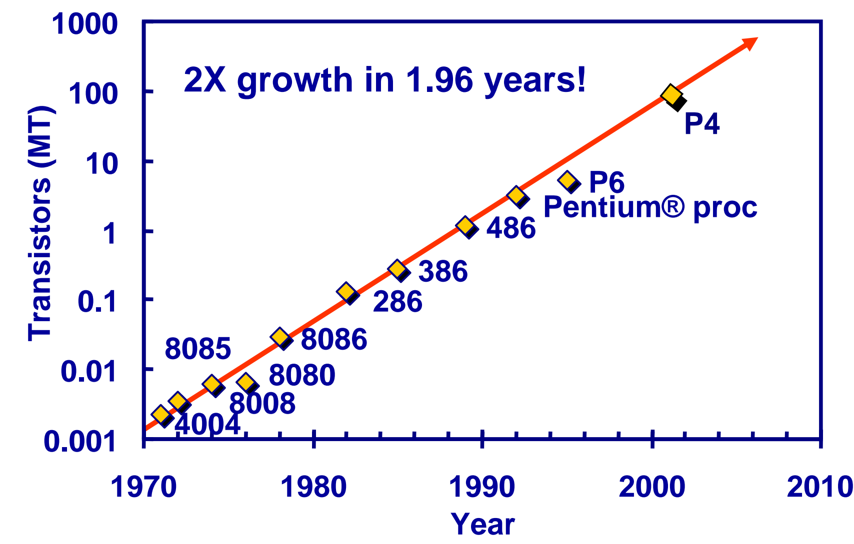
Evolution in Complexity



Transistor Counts

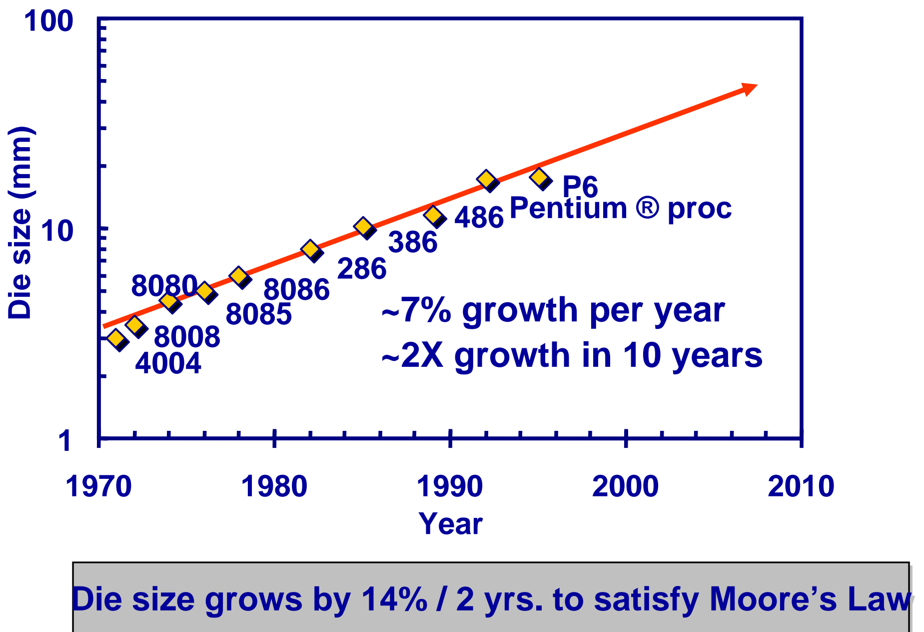


Moore's law in Microprocessors



Transistors on Lead Microprocessors double every 2 years

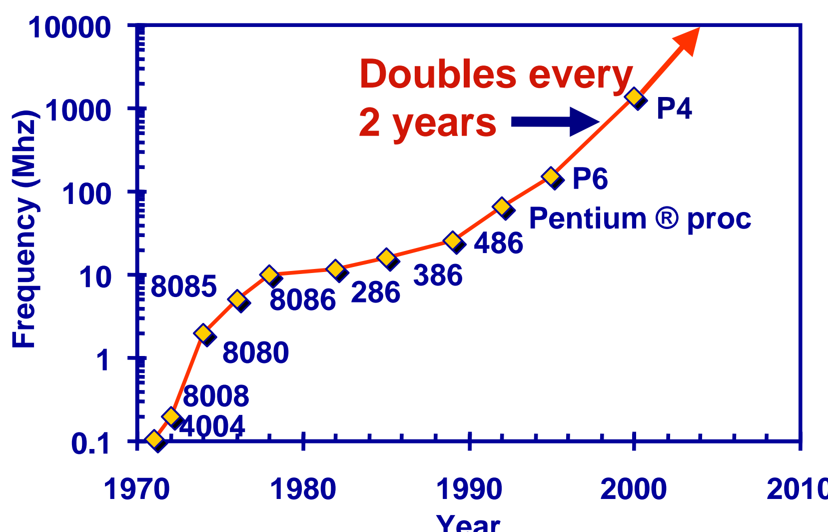
Die Size Growth



Die size grows by 14% / 2 yrs. to satisfy Moore's Law

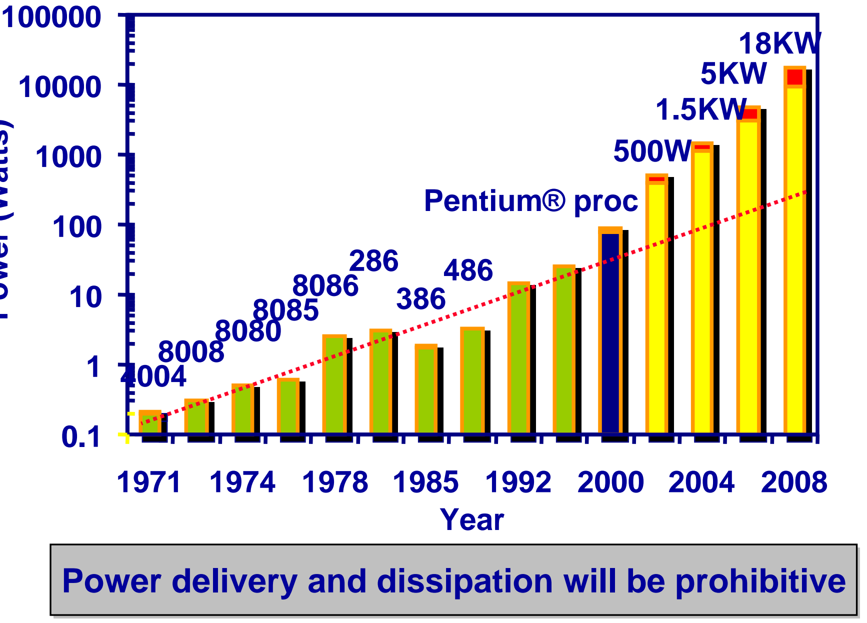
Courtesy, Intel

Frequency



Lead Microprocessors frequency doubles every 2 years
Transistors on Lead Microprocessors double every 2 years
Die size grows by 14% / 2 yrs.

Power will be a major problem

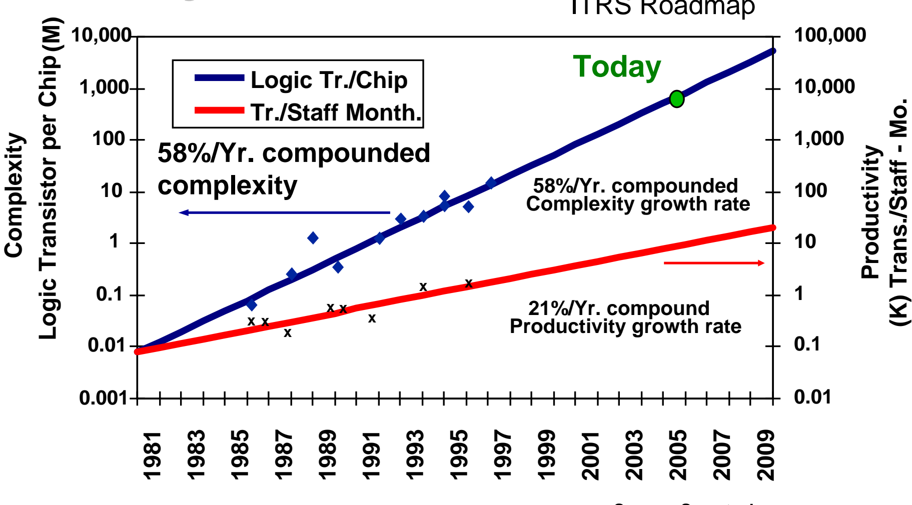


Power delivery and dissipation will be prohibitive

Courtesy, Intel

Productivity Trends

ITRS Roadmap



Source: Sematech

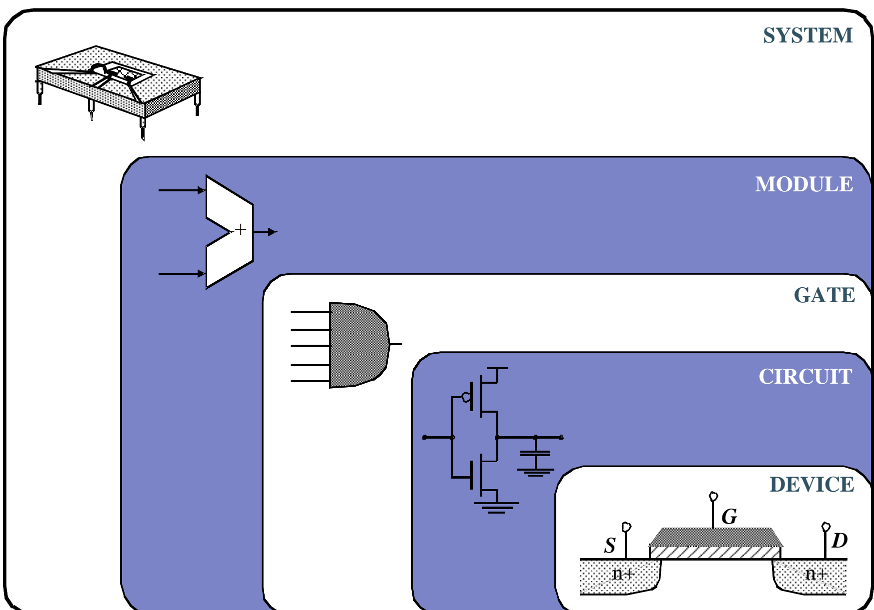
- Electronic design automation (EDA) tools to deal with complexity.
  - Cadence

Why Scaling?

- Technology shrinks by 0.7/generation
  - **# of transistors / die doubles every 2 years.**
  - **Can integrate 2x more functions per chip.**
  - **Cost per function decreases by 2x.**
- Main problem: power delivery and dissipation.

- How to design more and more complex chips?
  - Designer productivity does not double every two years.
  - Understand and exploit different levels of abstraction.
  - Automated tools (EDA).

Design Abstraction Levels



Started with large scale – microprosesors.

Go down to gate level, transistor level, then back up.

2010 Outlook

- Performance 2x / 2 years
  - 1 T (Tera) instructions / s
  - 20 – 30 GHz clock
- Complexity
  - # transistors: 1 Billion
  - Die area: 40mm x 40mm
- Power
  - 10 kW !
  - Leakage: 1/3 of total power

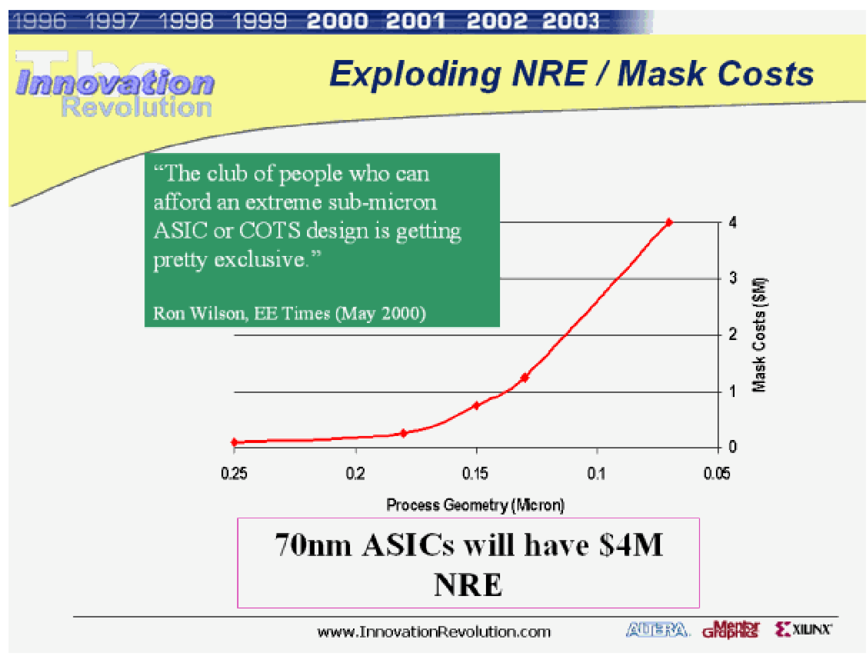
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
- Outline
  - **Cost**
  - Reliability
  - Speed
  - Power

Cost of Integrated Circuits

- NRE (Non-Recurrent Engineering) costs - fixed
  - Design time and effort, mask generation
    - Independent of sales volume / number of products
    - One-time cost factor
  - Indirect costs (company overhead)
    - R&D, manufacturing equipment (Fab), etc.
- Recurrent costs - variable
  - silicon processing, packaging, test
    - proportional to **volume**
    - proportional to **chip area**

NRE Cost is Increasing



Total Cost

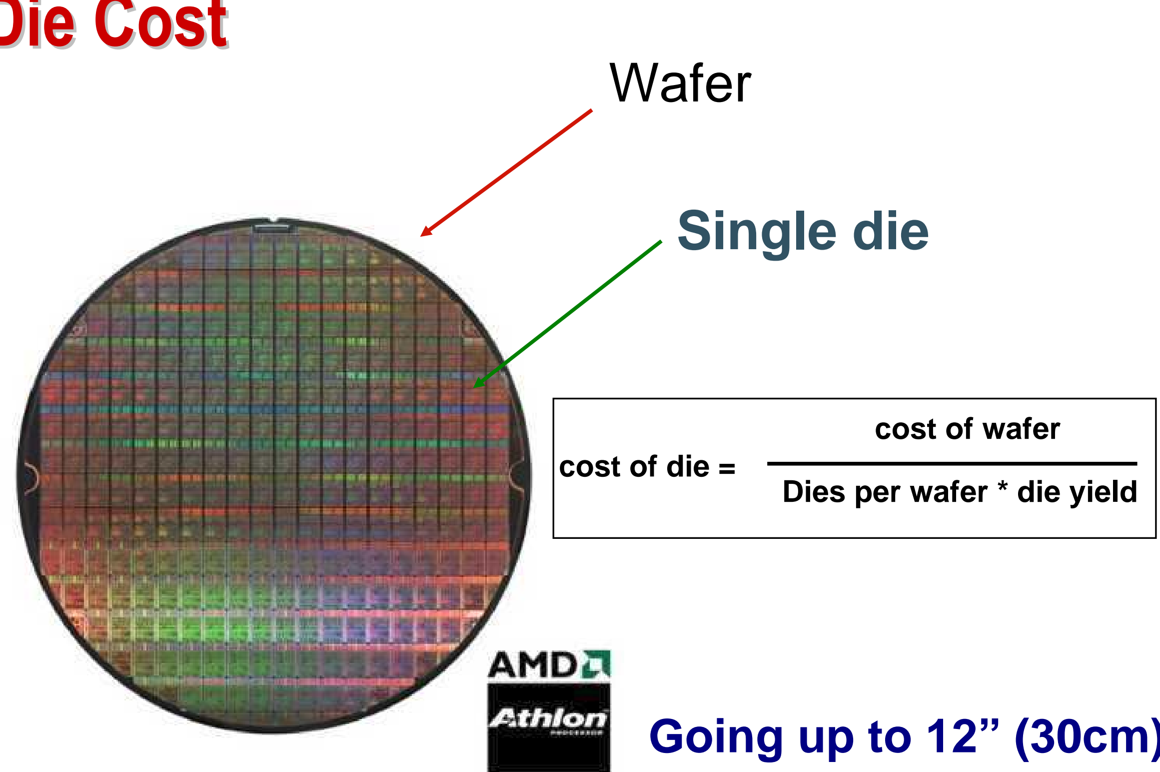
- Cost per IC

$$\text{Cost per IC} = \underbrace{\text{variable cost per IC}} + \frac{\text{fixed cost}}{\text{volume}}$$

- Variable cost

$$\text{Variable cost} = \frac{\text{cost of die + cost of die test + cost of packaging}}{\text{final test yield}}$$

Die Cost



$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{Dies per wafer * die yield}}$$

Going up to 12" (30cm)
8 – 12 "

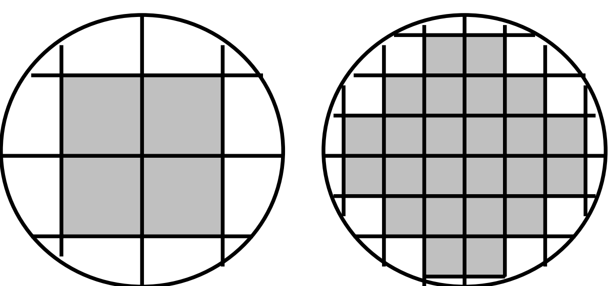
From http://www.amd.com

Yield

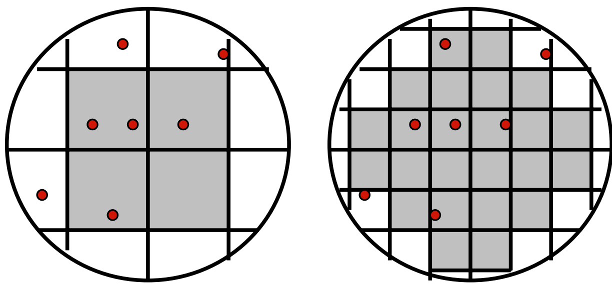
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

$\alpha \approx 3$, complexity of mfg. process

Defects per unit area = 0.5 – 1 / cm^2

die cost = *f* (die area)^4

die cost = f(die area)^4

$$\text{die cost} = \frac{\text{Wafer cost}}{\text{dies per wafer} \times \text{Die yield}}$$

$$\text{dies per wafer} \propto \frac{1}{\text{die area}}$$

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha} \qquad \alpha = 3$$

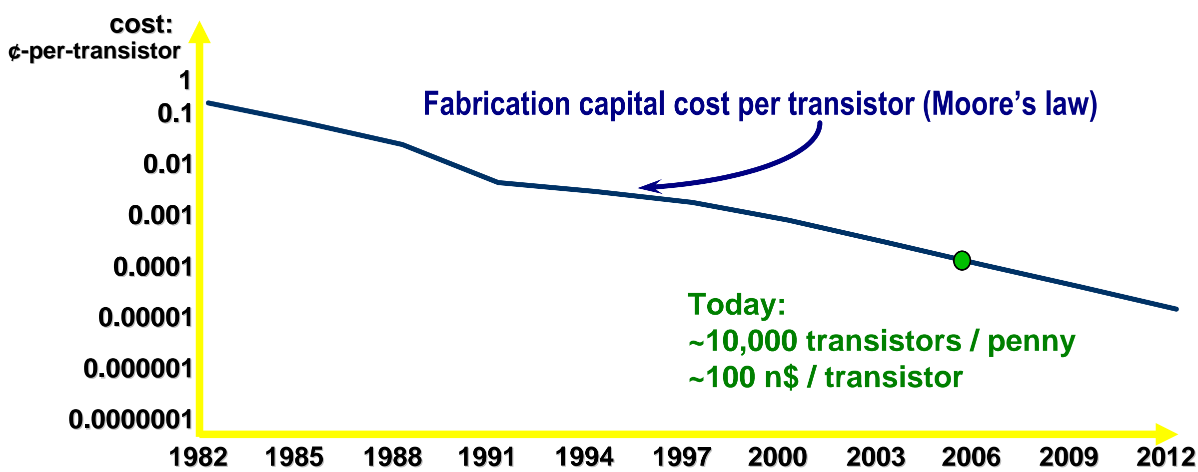
$$\text{die yield} \propto \left(\frac{1}{\text{die area}}\right)^3$$

$$\text{die cost} \propto (\text{die area})^4$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

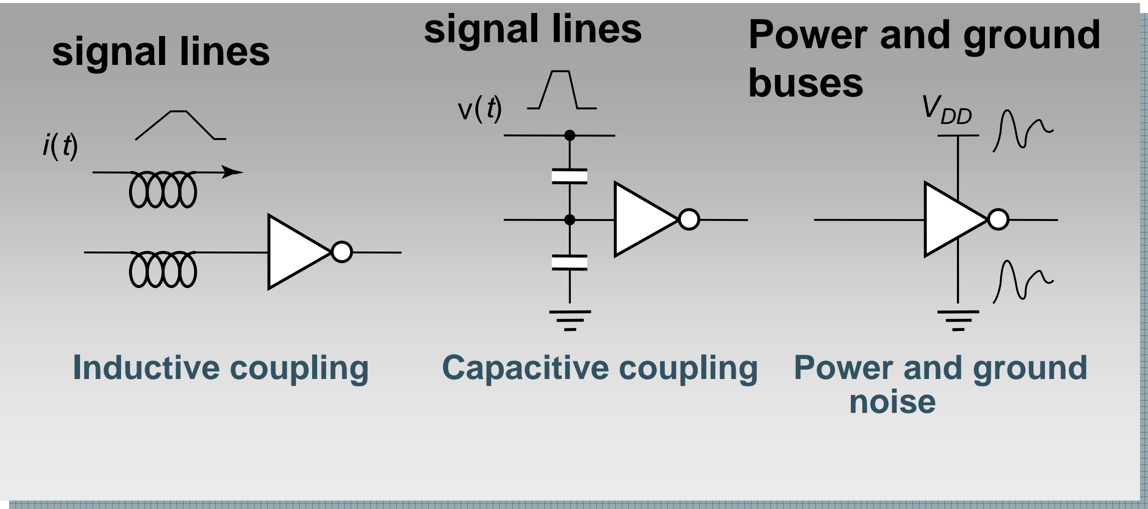
Cost per Transistor



Outline

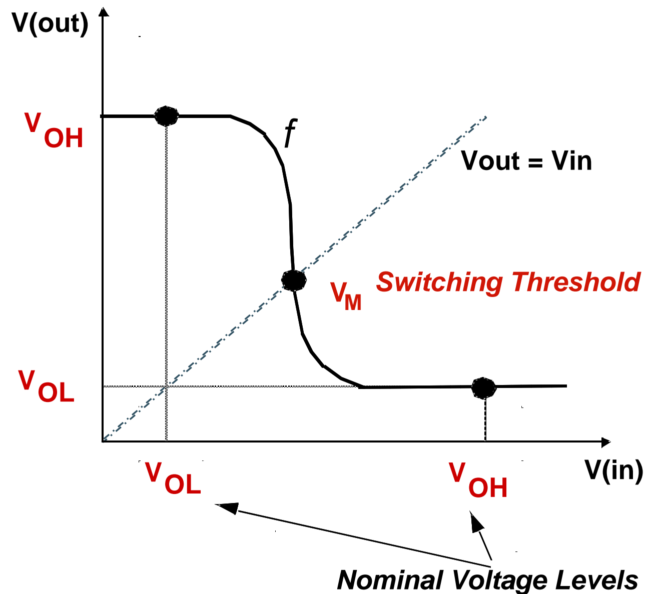
- Design Metrics
  - Cost
  - **Reliability - Noise**
  - Speed
  - Power

Reliability — Noise in Digital Integrated Circuits



- **Noise sources**
  - Internal (proportional to signal swing)
  - External (not related to signal levels)

DC Operation
Voltage Transfer Characteristic

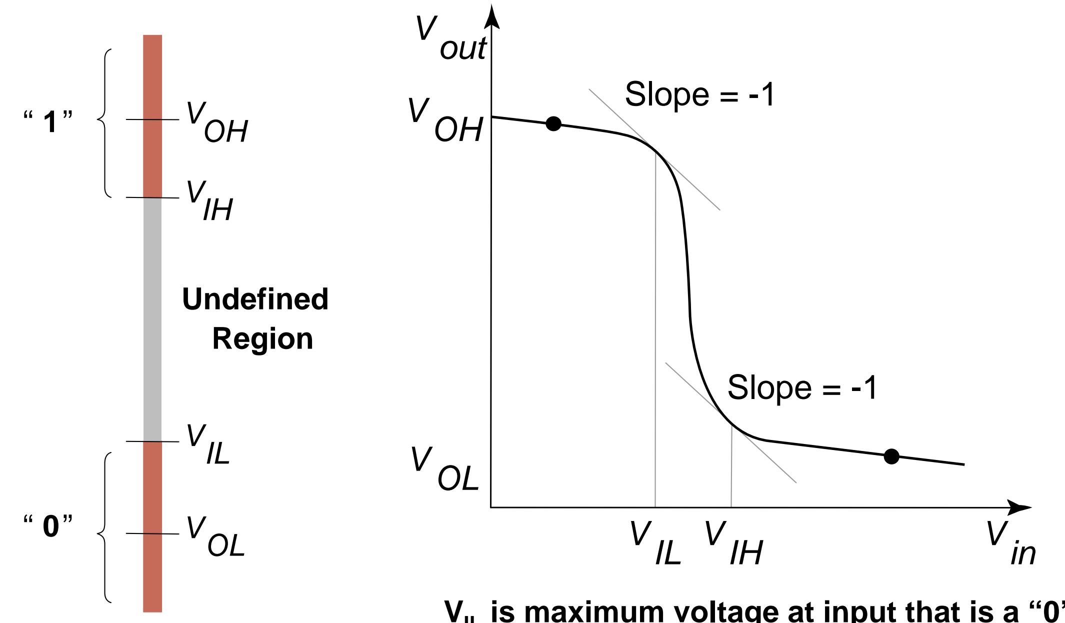


$V_{OH} = f(V_{OL})$
$V_{OL} = f(V_{OH})$
$V_M = f(V_M)$

$V_{OH} = V_{Out\ High}$
$V_{OL} = V_{Out\ Low}$
V_M = Switching threshold
V_{sw} = Signal swing = $V_{OH} - V_{OL}$

How much can input signal deviate from V_{OH} and V_{OL} and circuit still work?

Mapping between analog and digital signals

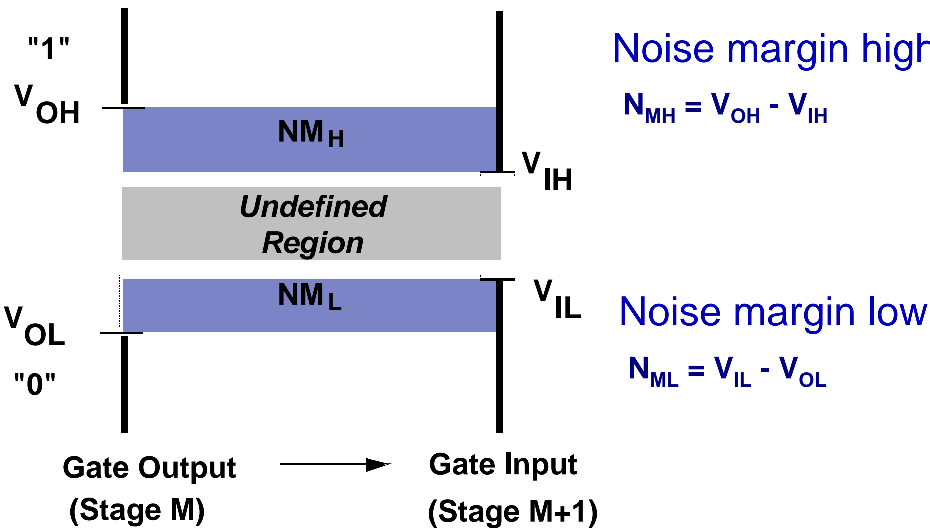


V_{IL} is maximum voltage at input that is a "0".
V_{IH} is minimum voltage at input that is a "1".
In between is undefined.

$V_{IL} = V_{input\ low}$

$V_{IH} = V_{input\ high}$

Definition of Noise Margins



Noise margin high

$N_{MH} = V_{OH} - V_{IH}$

Noise margin low

$N_{ML} = V_{IL} - V_{OL}$

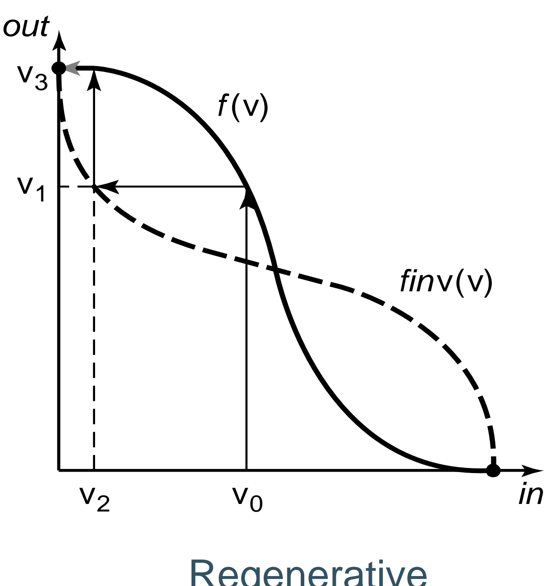
Noise Budget

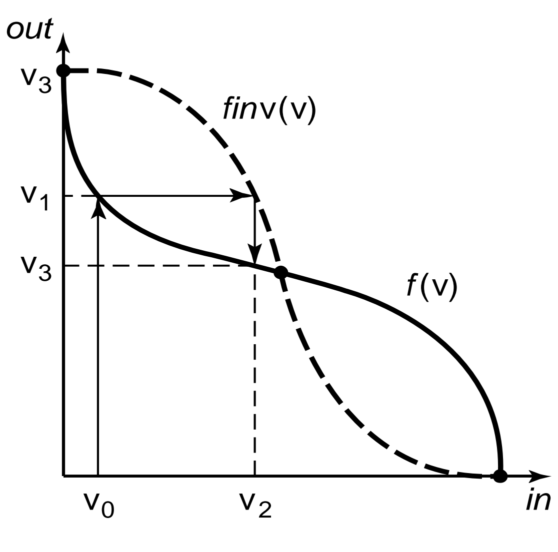
- Allocates gross noise margin to expected sources of noise
- Sources:
  - power supply (noise on power supply / ground)
  - offset
  - cross talk (inductive and capacitance)
  - Interference (consequtive signals)
  - Timing (jitter and skew)
- Differentiate between fixed and proportional noise sources

Key Reliability Properties

- **Absolute noise margin values are deceptive**
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- **Noise immunity is the more important metric – the capability to suppress noise sources**
- **Key metrics:**
  - Noise transfer functions
  - Output impedance of the driver
  - Input impedance of the receiver

Regenerative Property



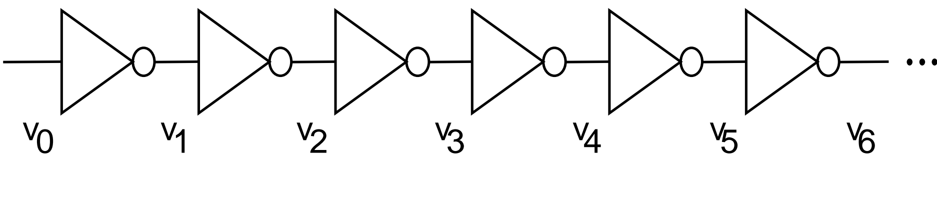


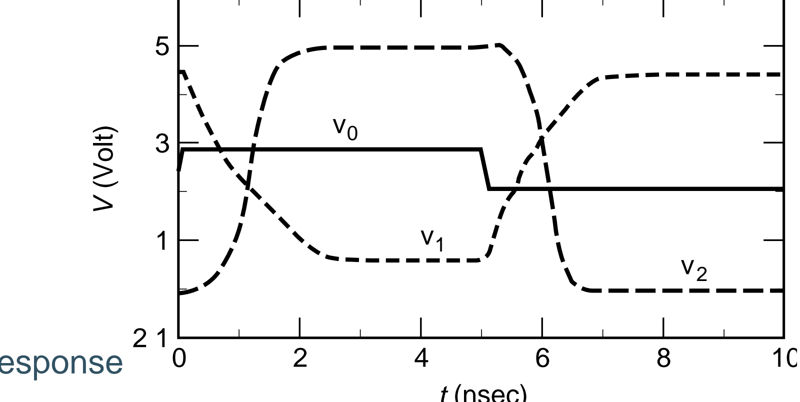
Regenerative

Non-Regenerative

Regenerative Property

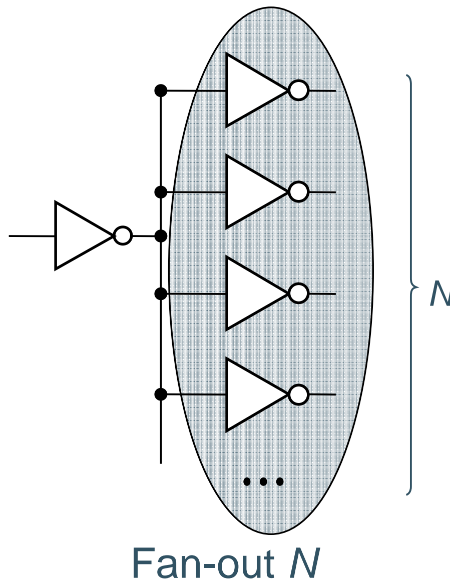
A chain of inverters

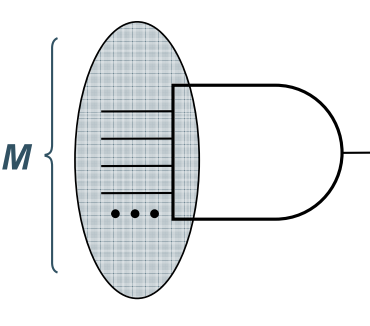




Simulated response

Fan-in and Fan-out

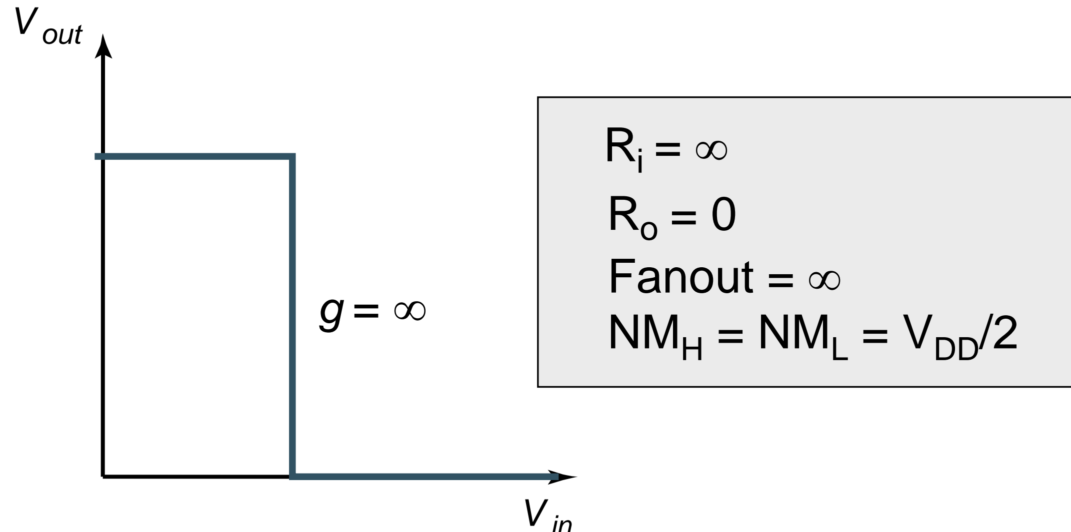




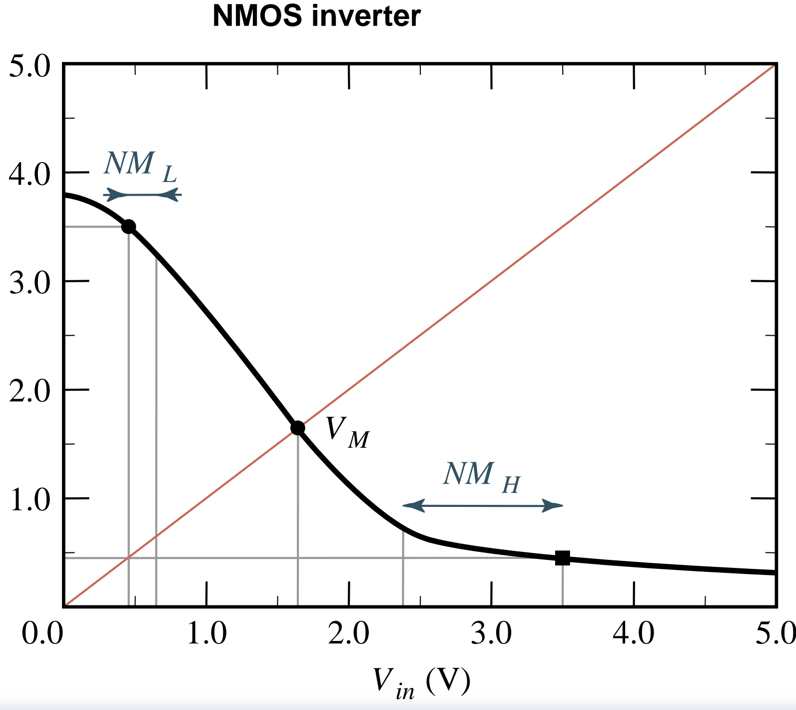
Fan-out N

Fan-in M

The Ideal Gate



An Old-time Inverter



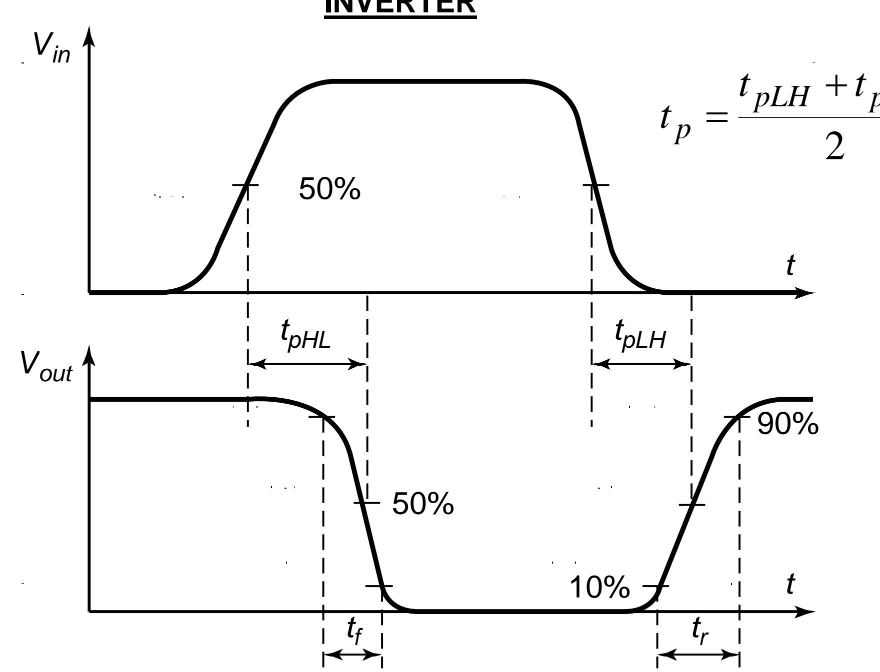
Outline

- Design Metrics
  - Cost
  - Reliability - Noise
  - **Speed**
  - Power

Delay Definitions

INVERTER

Defined
w.r.t. output



$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Lot of output loading C_L increast t_f and t_r

Delay Definitions

t_{pHL} – output high to low delay time

t_{pLH} –output low to high delay time

t_p – propagation delay

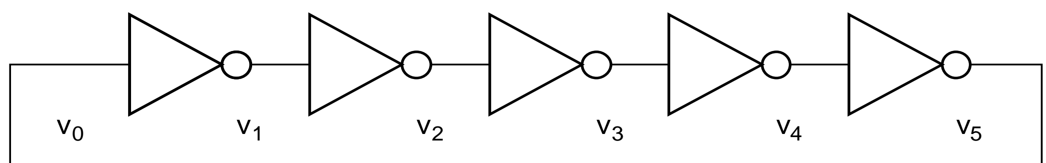
t_r – rise time

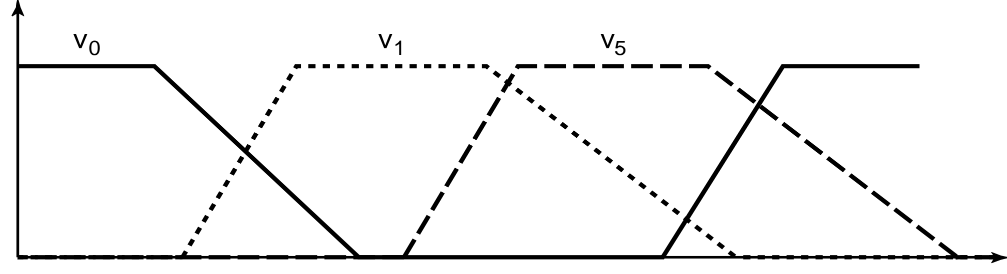
t_f – fall time

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

t_p is an mostly used to compare different technologies. Artificial metric.

Ring Oscillator – measuring t_p





$$T = 2 \times t_p \times N$$

A First-Order RC Network

R
Vout
Vin
C

$$v_{out}(t) = (1 - e^{-t/\tau})\, V_{in}$$

$t_p = \ln(2)\, \tau = 0.69\, RC$

Delay: 0.69 RC
90% poing: 2.2 RC

Important model – matches delay of inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}\ i(t)$$

Peak power:

$$P_{peak} = V_{supply}\, i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

Energy and Energy-Delay

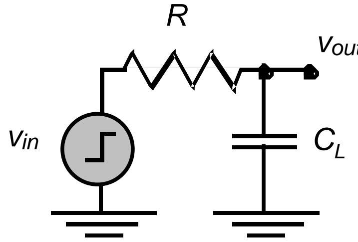
Power-Delay Product (PDP) =

E = **Energy per operation** = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

A First-Order RC Network



$$E_{0\rightarrow 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$

Summary

- **Digital integrated circuits have come a long way and still have quite some potential left for the coming decades**
- **Some interesting challenges ahead**
  - Get a clear perspective on the challenges and potential solutions
- **Understand the design metrics that govern digital design**
  - Cost, reliability, speed, power and energy dissipation