EE 134 HW3 due Thurs. Mar. 2

1. Delay time through an inverter:

Calculate the average propagation delay time (t_p) through a minimum size inverter driving an identical minimum size inverter using the example process of the text. This corresponds to an inverter similar to Fig. 5-15. The difference is that both the NMOSFET and PMOSFET have W/L = 0.375 / 0.25.

a. For the PMOS, scale the values for the capacitances in Table 5-2.

b. Determine the appropriate values of $R_{eq,p}$ and $R_{eq,n}$.

c. Determine t_{pHL}, t_{pLH}, and t_p.

2. Design a chain of inverters to drive a large capacitive load:

The output of an inverter sized as shown in Fig. 5-15 must be sent to an output pin with a capacitance of 20 pF. The average maximum delay is specified to be less than 2 ns. Design an inverter chain that uses the fewest number of inverters and still meets the delay specification. Use parameters for the example process of the text.

3. Design a static complementary CMOS logic gate:

Design a complementary CMOS logic gate to implement the logic Y = AB(C+DE). (you can assume that you will have an inverter available at the output).

a. Draw the circuit schematic so that there is minimum capacitance at the output node.

b. Assuming all minimum size inverters (identical to that in problem 1), calculate the worst case t_{pHL} and t_{pLH} for C_L = 50 fF neglecting all other capacitance. Use the first order approximation that we used in class of 0.69 R_{eq} $C_{L.}$