EE134 HW 2

Designing at the transistor level, requires an intuitive understanding of the transistor operation for the particular technology for which you are designing, i.e. HP06, AMI C5N, etc. All of the examples in the text are for a 0.25 μm process with V_{DD} = 2.5V. The HP06 process for which you are designing is a 0.6 μm process with V_{DD} = 5V. Since the voltages scale like the lengths, we should expect to see velocity saturation. In this homework, you will see the effect of velocity saturation for yourself. You will find the parameters (Table 3-2) for the unified current model (Fig. 3-23) to fit our FETs. You will find the equivalent resistances, $R_{eq,n}$ and $R_{eq,p}$ (Eq. 3.43), for our FETs.

We will start by comparing the current voltage relations of two FETs with the same W/L ratios. FET 1 has W/L = 0.9 / 0.6 and FET 2 has W/L = 13.5 / 9. (All length units are in microns)

1. Set V_{DD} = 5V. Calculate, plot, and save the numerical output (for later) for
(a) (NMOSFET) I_D versus V_{GS} (0 – 5V) for both W/L sizes.
(b) (PMOSFET) I_S versus V_{SG} (0 – 5V) for both W/L sizes.
Turn in one plot each for (a) and (b). Plots should look like this.

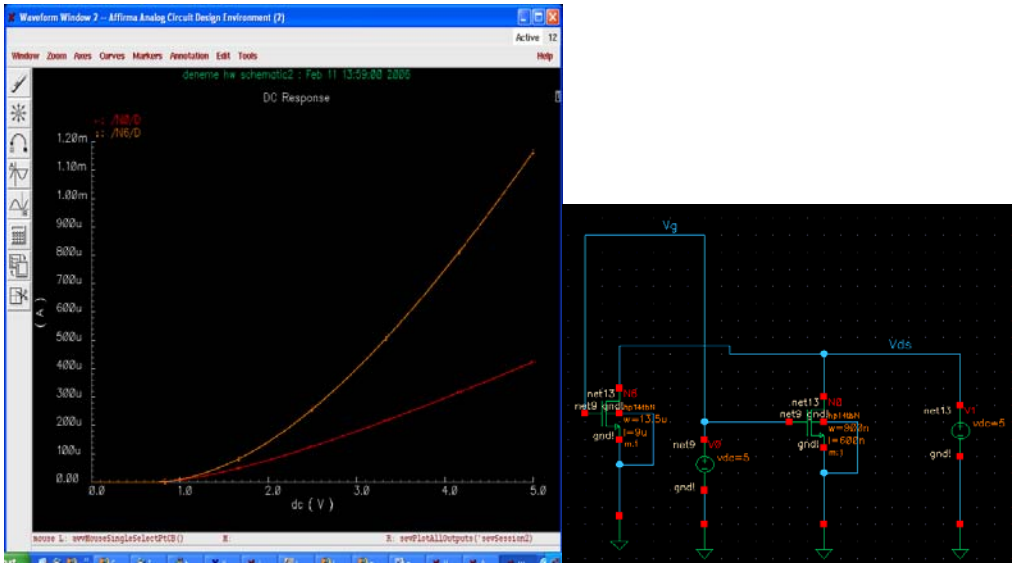

Fig. 1. (a) Plot of NMOS I_D vs. V_{GS}. (red) W/L=0.9/0.6. (orange) W/L = 13.5/9. (b)The schematic to be used for comparison. Two different size transistors, with common V_{GS} and V_{DS}, where V_{GS} is swept.

Discuss why the two curves are different. Use mathematical equations whenever possible to make your point.

2. For a W/L = 0.9 / 0.6 NMOS and PMOS do the following. For 5 different values {1V, 2V, 3V, 4V, 5V} of V_{GS} (NMOS) and V_{SG} (PMOS), sweep V_{DS} (NMOS) and V_{SD} (PMOS) from 0 – 5V in increments of 0.1V. Turn in one plot for the PMOSFET and one plot for the NMOSFET. The plots should look like this.

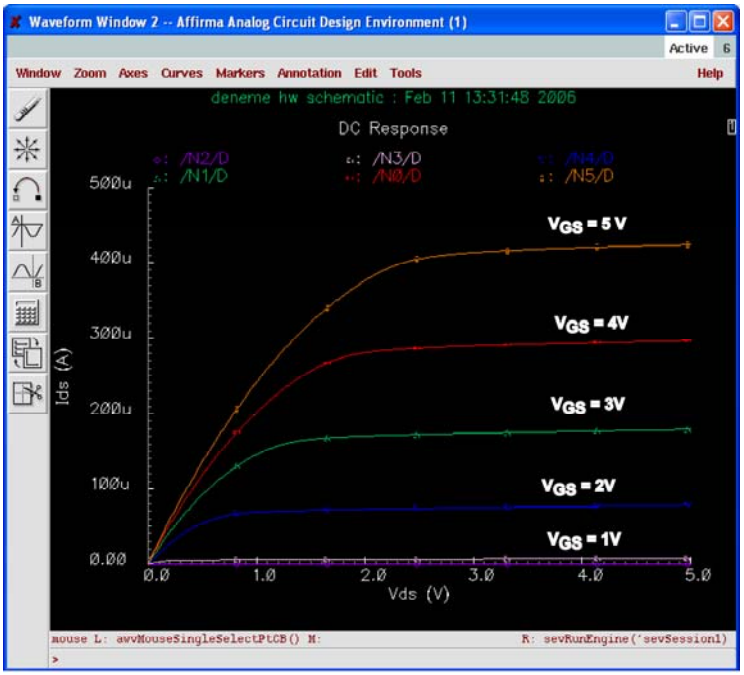

Fig. 2. NMOSFET I_D vs. V_{DS} for V_{GS} = {1V, 2V, 3V, 4V, 5V}.

Save the numerical data for later. You will fit to it using MATLAB to produce a figure like Fig. 3-25 of the text. There are 2 ways that I know of to make the plot of Fig. 2. One way is to do 5 separate runs with 5 values of V_{GS}, keep the numerical output, and overlay the plots in MATLAB. Another way is to create a circuit like the one shown below where each FET has a different V_{GS}.

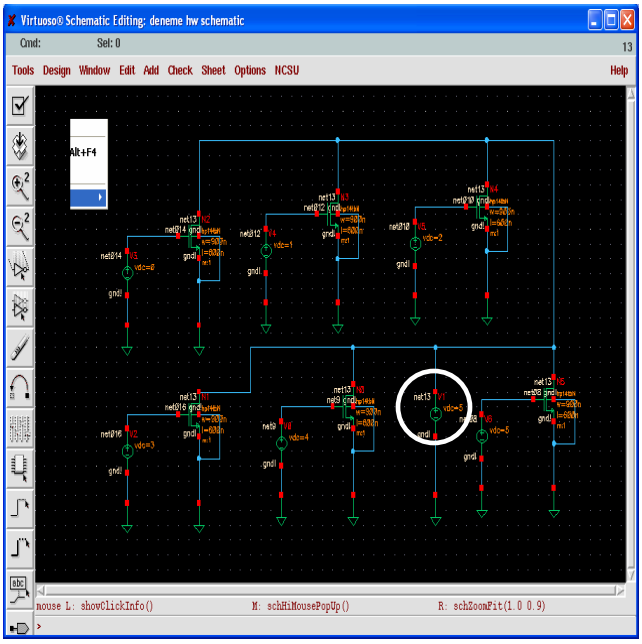

Fig. 3. Circuit used to create Fig. 2. The Source in the white circle is the common Vds which should be swept for the simulation

3. Using the data from problem 2 and the data generated in problem 1 for the W/L = 0.9/0.6 devices, determine parameters for the unified model for your NMOSFET and PMOSFET. Create a table corresponding to Table 3-2.

A good place to start is with the Level 3 SPICE parameters found here

http://www.ee.ucr.edu/~rlake/EE135/t15d-params.doc

You can find values for VTO and KP. For V_{DSAT}, as a start, try multiplying the values in Table 3-2 by 2 since that will make the electric fields in your device similar to those in the 0.25 μm device. λ is simply the slope of the $I_D - V_{DS}$ curve in saturation. You can read GAMMA directly off from the Level 3 SPICE parameters.

If you have to emphasize one curve to fit very well, for NMOS fit the $I_D - V_{DS}$ curve with V_{GS} = 5V and for PMOS, fit the $I_S - V_{SD}$ curve with V_{SG} = 5V.

Once you have a good fit, proceed to 4.

4. Calculate $R_{eq,n}$ and $R_{eq,p}$ for your FETs both <u>numerically</u> and <u>analytically</u> using your new model. For the analytical calculation, use Eq. (3.43). For the numerical calculation, simply average the 2 resistances as illustrated in Fig. 3-27b.