EE 134 HW1 due Tues. Feb. 7

1. Sketch the cross-section of a CMOS transistor pair and label all of the layers.

2. In the cross-section of 1, draw in the parasitic diodes and capacitors at each pn junction. Draw the diode symbols with the correct polarity.

3. Should the bias of the p-Si substrate be higher or lower than the bias on the n-wells or n-select regions. Why?

4. Should the n-well be tied to ground (the lowest voltage on chip), V_{DD} (the highest voltage on chip), or left floating? Why (consider the standard biasing of a PMOS transistor in a CMOS inverter)?

5. Explain the difference between a long channel transistor and a modern short channel transistor.

6. For VDD = 2.5 V and the inverse subthreshold slope S = 100 mV/dec at T=300K, what is the maximum on-off current ratio of the transistor? What is the maximum on-off current ratio at 100^{o}C?

7. For the model process used in the text (using parameters from Table 3.2 and V_{DD} = 2.5V), calculate the W_p/W_n ratio of a CMOS inverter for a switching threshold of
   a. 1 V
   b. 1.5 V

   At the end of each calculation, show that you used the correct value of V_{min} from Figure 3-23.