Single electron memory devices: Toward background charge insensitive operation

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We present an experimental study of charging mechanisms in aluminum single electron memory cells where the SiO_2 surface between the floating gate and the control gate is used as a barrier dielectric and the single electron transistor is used as a readout device. We study several regimes of charging for different barriers separating the floating gate and the control gate. For thinner barriers, the floating gate acts as a single electron trap, while for thicker barriers a few tens of electrons could be stored on the floating gate to represent a bit. This allows us to realize a background charge insensitive operation of the memory cell. In devices with a barrier thickness in the range 30–100 nm we observe no charge transfer to the floating gate, but rather charging of the surface traps present in the barrier. Our results are in good agreement with theoretical calculations where specific details of device geometry are included in the model.
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I. INTRODUCTION

Single electron effects will come to play an important role as semiconductor device dimensions are scaled down to follow the exponential improvement in the density and performance, as characterized by Moore's law. Coulomb blockade effects have been utilized to demonstrate a number of devices.[1,2] These devices can be scaled down to atomic dimensions, enabling integrated circuits of terabit densities, along with high speed and low power dissipation. However, a number of problems need to be addressed for the emergence of practical room temperature integrated single electron devices. Room temperature operation necessitates an extremely small feature size of a few nanometers. Hence the development of lithographic techniques for nanometer dimensions is eagerly awaited. Another important problem which has to be solved is the problem of random background charge (Q_0). Single electron devices being extremely sensitive to external charge, their switching thresholds are easily shifted by the random charging of nearby traps (which induce random offset charges), resulting in a high probability of errors which cannot be corrected by known redundancy schemes.[1,2]

Recently, methods to overcome this problem for single electron memories have been proposed.[3,4] In the first method,[3] the data bit is represented by the excess or shortfall of a small amount of charge transferred by means of tunneling from a control gate (CG) to a floating gate (FG). To readout the memory state, a single electron transistor (SET) is used. This proposed memory cell is analogous to present day flash memory cells with the SET used in place of the field-effect transistor (FET), and it can be considered to be the ultimate destination of the present day flash memory cell. By applying an appropriate voltage between the word line and the bit lines (the SET is connected between the bit lines), either a logic zero or a logic one can be written on to the FG. Read out is done by writing a logic zero. If the initial state is a logic zero, there will be no change in the charge on the FG, consequently the current through the SET remains constant. Alternately, if the initial state is a logic one, there will be an erasure of this bit leading to Coulomb blockade oscillations in the SET, which are amplified and rectified to give the output. In this way, a destructive readout of the stored bit is used to overcome the problem of random background charge. Here the initial working point of the SET electrometer does not matter, for it changes only the phase of the oscillations.

In the second method,[4] an additional FG (compensation FG) also coupled to the SET electrometer, is used to store an adjustable charge through a separate word line. This ''compensation'' charge is set periodically to nullify the offset charge induced by random background charge fluctuations.

A low temperature prototype of a memory cell based on the first method[3] was fabricated and characterized by Chen *et al.*,[5] where the FG was charged from a CG placed 20–30 nm away. The current through the SET began oscillating upon ramping up/down the CG bias beyond a threshold value. A cancellation voltage was applied to the back gate to negate the direct influence of the CG bias on the SET electrometer.[5] These continuous oscillations were attributed to the charging of the FG by Fowler–Nordheim tunneling, thus changing its potential.

However, several discrepancies with the explanation proposed in Ref. 5 become apparent on a closer look. Considering the size of the FG and the coupling capacitances, the transfer of even a single electron to/from the FG should lead to a discrete change in the conductance through the SET, unlike the continuous change seen.[5] Such a discrete change

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in the conductance has been seen in experiments with Al/AlO_x single electron traps, and silicon single electron memory cells.[6,7] Also each oscillation in the detector during charging should comprise of a few electrons transferred to/from the FG. These observations lead one to infer that it may not be the charging of FG rather some other charging mechanism which led to the results seen by Chen *et al.*[5]

We report here measurements on FG single electron memory cells with different barriers between the CG and the FG. We also report on measurements on cells without a FG. These cells are specifically fabricated to see if other charging mechanisms get activated on the application of a high CG bias.

II. FABRICATION

Devices are fabricated on SiO_2 substrates using electron beam lithography on a bilayer resist and double angle evaporation of aluminum, with *in situ* oxidation.[8] By appropriately positioning the FG laterally with respect to the CG and the SET, the barrier to electron tunneling and the strength of electrometer coupling can be varied to study charging in different tunneling regimes (low electric field and high electric field). Measurements are performed in a He^3 cryostat in the temperature range 300 mK–3 K, limited by the operating temperature of our SET detectors whose charging energy (E_c) is about 1 meV. Conductance of the SET detectors is measured using standard lock-in techniques at a frequency of 17 Hz with an excitation voltage of 100 μV. A magnetic field of 1 T is applied to suppress the superconductivity of aluminum.

III. EXPERIMENTS AND DISCUSSION

The width of the tunnel barrier is an important parameter in memory devices for it determines the time taken to transfer charge on to the FG and its retention time, processes which demand opposing requirements on the tunnel barrier width. We present experimental results for single electron memory cells which operate in the ''one or few electrons per bit'' storage mode using regular tunneling (not requiring any significant electric field). A schematic circuit diagram of the device is shown in Fig. 1(a). The scanning electron microscope micrographs of two devices ''A'' and ''B,'' having different gaps between the FG and the CG, are shown in Figs. 1(b) and 1(c), respectively. The SiO_2 surface in the lateral gap between the FG and the CG is used as a barrier dielectric. The application of a CG bias leads to a higher probability of an electron transfer to occur between the CG and the FG by tunneling through several nm of SiO_2. This applied bias also induces an external charge on the SET island leading to Coulomb blockade oscillations in the SET. To clearly distinguish the effect of the charging of FG on the conductance of the SET, an opposing bias is applied to the back gate to cancel the control gate induced external charge thereby suppressing the Coulomb blockade oscillations in the SET.[9] The back gate bias for a complete cancellation (''flat cancellation) is $V_{bg} = -\gamma V_{cg}$, where V_{cg} is the applied CG bias and $\gamma = C_{cg}/C_{bg}$, C_{cg}, and C_{bg} are the coupling capacitances

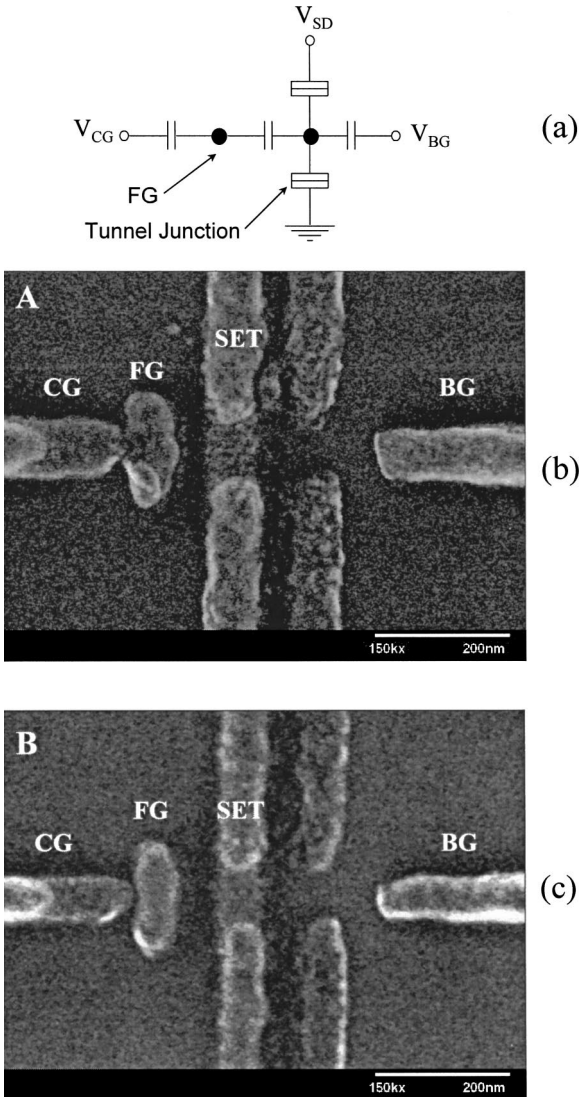

FIG. 1. Floating gate single electron memory cell: (a) schematic circuit diagram of the device and, SEM micrographs of two narrow gap devices, (b) device ''A'' with a gap ~4 nm between the CG and the FG, and (c) device ''B'' with a gap ~8 nm between CG and FG.

from the control gate and the back gate to the SET, respectively. In ''flat'' cancellation the conductance through the SET does not change on varying the CG bias until an electron is transferred to/from the FG. This changes the potential on the FG and on the SET island, which not being cancelled by the back gate, causes a change in the conductance through the SET.

Figure 2(a) shows the conductance through the SET as the CG bias is swept in two directions with ''flat'' cancellation by the back gate in device ''A.'' As the electron population on the FG is sequentially changed, the conductance through the SET changes in a step wise fashion, with the envelope of the response characteristic following the outline of the electrometer's oscillations. The number of steps per oscillation depends on the size of the FG and on the strength of coupling between the FG and the electrometer. We observe five steps per oscillation in device ''A'' with a sixth step hidden in the insensitive region at peak conductance. This result is in

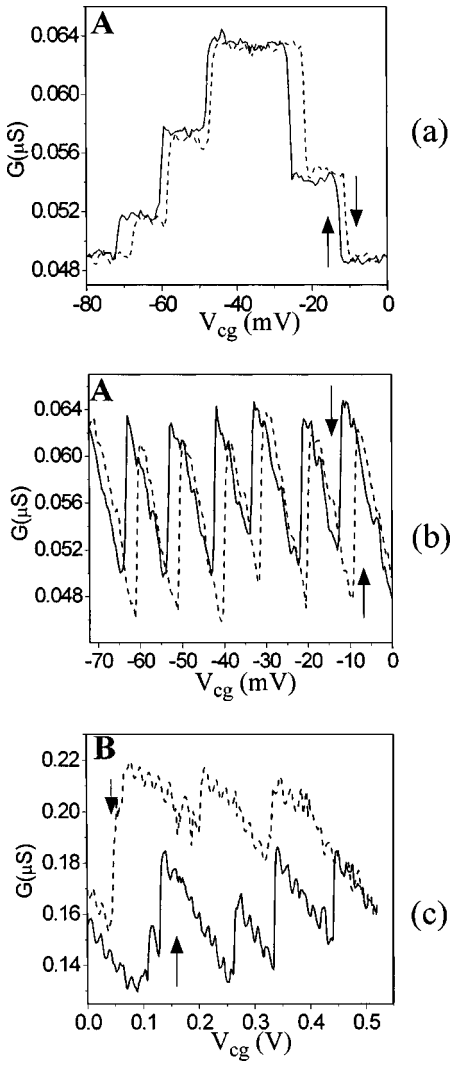

FIG. 2. SET electrometer response as the CG voltage is swept in two directions: (a) in device "A" with "flat" cancellation by the back gate and (b) with "over" cancellation by the back gate. The arrows represent the direction of the change in the SET bias point, on an electron transfer to (from) the FG corresponding to the solid line trace (dashed line). (c) The response in device "B" with "over" cancellation showing better hysteresis loops obtained due to a thicker barrier.

very good agreement with simulations performed for the particular device geometry using FASTCAP,[10] which give the same number of electron transfers per period of oscillation.

The advantage of "flat" cancellation is that the charging/discharging of the floating gate is detected by oscillations in the SET conductance. However, different electron transfer events change the SET conductance by different amounts. To achieve the same magnitude of change in the SET response for each electron transfer event, "over" cancellation by the back gate is used in which the magnitude of the external charge induced by the back gate is greater than that induced by the CG. This technique resets the operating point of the SET when a change is caused by an electron transfer to/from the FG, leading to saw tooth oscillations in the electrometer.

Figures 2(b) and 2(c) show the conductance response of the SET as the CG bias is swept in two directions with "over" cancellation by the back gate for devices "A" and "B," respectively. Abrupt jumps can be seen which correspond to single-electron charging/discharging of the FG. As can be expected, device "A" with a gap size of a few nm (<4 nm) has a significantly lower threshold for tunneling and a smaller hysteresis loop size than device "B," where the gap is about 8 nm. We can also see a strong correlation between the position of the electron transfer events in Figs. 2(a) and 2(b) for the "flat" and "over" cancellation techniques are essentially two different ways of representing similar data.

The memory effect exhibited by devices "A" and "B" is not strong enough for these devices to be used as nonvolatile memory cells. When the CG bias is reset to zero, at most one electron remains trapped on the FG due to a high rate of tunneling through the thin barriers. A nonvolatile memory cell (background charge insensitive device) requires several electrons to remain on the FG when the CG bias is reset to zero. Hence the barrier responsible for confining electrons on the FG has to be modified to prevent a quick discharge of the stored charge.

In another device "C," the FG is in close proximity to the SET island, rather than the CG. In this case, there is a higher probability of an electron tunneling between the FG and the SET island on the application of a CG bias. The increased coupling between the FG and the SET electrometer leads to a greater change in the SET conductance on a change in the electron population on the FG. The separation between the FG and the SET island is about 10 nm in this device. The CG is about 40 nm away from the FG.

Figure 3(a) shows a schematic diagram of the measured device. Figure 3(b) shows the sequential charge/discharge traces obtained on applying a CG bias of both polarities. To discharge the excess electrons stored on the FG in earlier traces, we apply a high negative voltage to the CG. Flat compensation is used and hence the electrometer conductance changes only with a change in the electron population on the FG. The barrier to tunneling present in this device is greater than the ones in other devices and it leads to the presence of a threshold voltage that has to be overcome for an electron to tunnel. After crossing the threshold, an electron transfer occurs from the FG to the SET island. This alters the potential on the FG changing the working point of the SET. A higher negative voltage on the CG discharges the FG further. Returning the CG voltage to zero does not charge the FG. A high positive voltage is required to do so. Similarly, returning the CG voltage to zero from a high positive voltage does not discharge the FG so excess electrons remain stored on the FG. A unit change in the electron population on the FG results in a change in the external charge on the SET island of about $e/2$, resulting in a shift in the working point of the SET by almost half a period. If the working point is set to a minimum in the gate modulation characteristic, an electron transfer event will cause it to switch to the maximum and vice versa. Setting the working point in the middle of the linear response region will lead to a very small change in the signal. Hence we have demonstrated a background charge

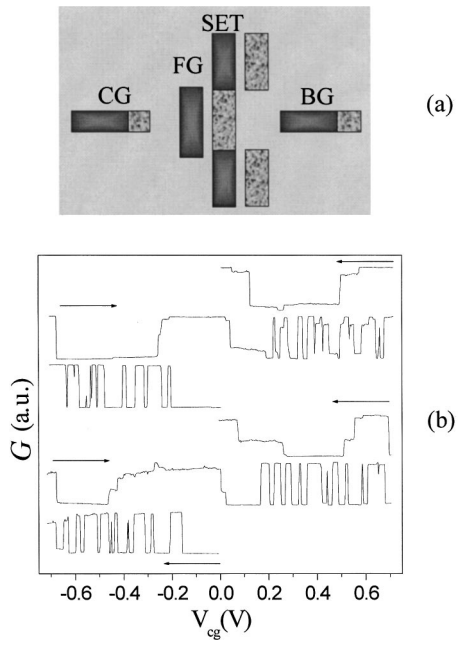

FIG. 3. Nonvolatile memory device: (a) schematic of the device, with FG closer to the SET island rather than the CG and (b) experimental results demonstrating the nonvolatile memory function of the device. The first reverse sweep discharges the electrons stored on the FG and resets the device. Subsequent forward sweep charges the FG, about 20 electrons for the applied CG bias. This measurement sequence is repeated, with the successive traces shifted upward for clarity.

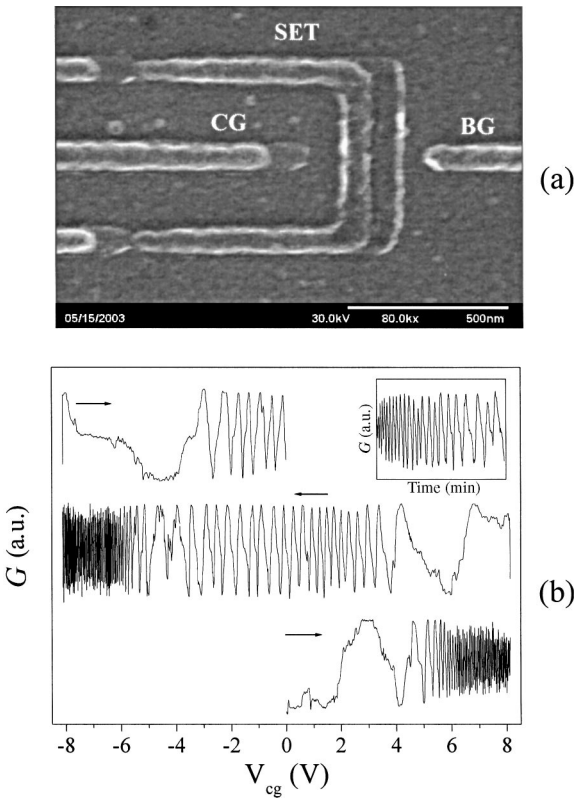

FIG. 4. Cell with no FG: (a) SEM micrograph and (b) the measured response of the electrometer on applying a high CG bias of both polarities with "flat" cancellation by the back gate. The oscillations at high bias are explained by the charging of the traps present in the oxide.

insensitive single electron memory based on a destructive readout of the stored memory bit.[3]

In an integrated circuit implementation of such a memory cell, a simple circuit can be added to count the number of single electron transitions, which indicate the storage or erasure of a bit. In our device, about 20–25 electrons are transferred each time a bit is stored on or erased from the FG (with an applied bias of ± 0.7 V). A few electron transfer events take place on the return traces but their number is significantly smaller (<5 events). This allows for a confident recognition of the memory status.

The experiments of Chen *et al.*[5] showed continuous oscillations in the SET at a high bias on exceeding a certain threshold. As was pointed out earlier and as will be demonstrated below, this charging cannot be that of the FG. This implies that another charge trapping mechanism becomes active at high bias conditions, and which needs to be investigated. Our experiments using devices with a large gap (30–100 nm) between the CG and the FG, show charging similar to that seen by Chen *et al.*[5] Also, a larger gap requires a higher threshold to be overcome, for the oscillations to begin. This continuous charging is related to the charging of traps present at the interface between the metal (aluminum) and SiO_2, and in the bulk and at the surface of SiO_2, and is not related to the FG. There is a large probability for the electrons being injected at high field in large gap devices to be trapped in these states. The collective charging and discharging of this "trap percolation network" can create an effect of a "moving electron cloud" causing continuous oscillations in the electrometer.

A similar charging behavior has been observed by Sunamura *et al.*[11] who have characterized a single electron memory cell which utilizes carrier traps in silicon nitride layer (memory node) coupled with an SET in a three layer memory structure. These traps were charged through the channel of a metal–oxide–semiconductor FET. The charging of these traps lead to continuous oscillations in the SET electrometer, as seen in large gap devices at high bias.

To further clarify the charging mechanism we have fabricated a cell consisting of an SET electrometer with a CG and a back gate, but with no FG. Figure 4(a) shows a micrograph of this cell. Figure 4(b) shows electrometer response curves obtained when the CG bias is ramped with a cancellation voltage applied to the back gate. If the trapping network is not present, and in the absence of a FG, the application of a CG bias with complete cancellation by back gate should result only in a constant current through the electrometer. We see that at small bias this is the case, however cancellation fails at high bias and the SET exhibits a number of continuous Coulomb blockade oscillations, as seen by Chen *et al.*[5] On further increasing the bias the rate of oscillations becomes more rapid and charging continues to occur even at a fixed bias albeit slowing with time [see inset in Fig. 4(b)]. These continuous oscillations can be explained by the charging of a trapping network as described earlier.

IV. CONCLUSIONS

We have demonstrated charging of the floating gate by regular tunneling in single electron memory cells with a small gap between the control gate and the floating gate. The change in electron population of the FG manifests as a periodic modulation of the electrometer conductance. We have demonstrated the first background charge insensitive memory in aluminum single electron FG memory cells operating in regular tunneling mode with a bit represented by about 20 electrons. We have studied charging seen in large gap devices at high bias conditions and propose a trapping network to be the cause of these oscillations. Further, charging of FG by FN tunneling remains to be seen. It is our view that the absence of surface traps makes it easier to study FN tunneling in stacked geometry devices than in lateral geometry devices. Further study using stacked geometry devices will hopefully shed more light on the feasibility of practical integrated single electron memory devices.

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[1]K. K. Likharev, Proc. IEEE **87**, 606 (1999).
[2]A. N. Korotkov, Int. J. Electron. **86**, 511 (1999).
[3]K. K. Likharev and A. N. Korotkov, Proceedings ISDRS, 1995, p. 355.
[4]A. N. Korotkov, J. Appl. Phys. **92**, 7291 (2002).
[5]C. D. Chen, Y. Nakamura, and J. S. Tsai, Appl. Phys. Lett. **71**, 2038 (1997).
[6]V. A. Krupenin, S. V. Lotkhov, and D. E. Presnov, JETP **84**, 190 (1997).
[7]N. J. Stone and H. Ahmed, Appl. Phys. Lett. **77**, 744 (2000).
[8]T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. **59**, 109 (1987).
[9]P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, and M. H. Devoret, Z. Phys. B: Condens. Matter **85**, 327 (1991).
[10]K. Nabors and J. White, IEEE Trans. Comput.-Aided Des. **10**, 1447 (1997).
[11]H. Sunamura, T. Sakamoto, Y. Nakamura, H. Kawaura, J. S. Tsai, and T. Baba, Appl. Phys. Lett. **74**, 3555 (1999).