

# Design and Optimization of ESD Lateral NPN Device in 14nm FinFET SOI CMOS Technology

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**50 Words Abstract** – We present the development of ESD lateral NPN device in 14nm FinFET SOI CMOS technology using body-contact and floating-body approaches. The effects of key design factors including base length, base doping, body resistance on the triggering and ESD performance of LNPN device are investigated to achieve an optimized design.

## I. Introduction

The Diode and Silicon-Controlled Rectifier (SCR) are typical ESD protection devices in advanced Silicon-on-Insulator (SOI) CMOS technologies. This is particularly true for I/O protection of low-voltage (e.g., < 1.0V) integrated circuits (ICs) where a relatively low trigger voltage for an ESD protection device is required. However, for the applications of mix-signal or high-voltage (e.g., 3.3V I/O) ICs, the design of ESD protection circuits needs to be tolerant of high voltage input signals. The turn-on voltage of single ESD diode is usually too low for such applications and the SCR with a holding voltage of ~1.2V can cause I/O latch-up issues. The stacked devices (e.g. diode string or diode in series with an SCR) may meet the design target but both result in a penalty of increased device area.

NFET-based devices were used as the solution of ESD protection for high voltage and low speed I/O applications in the previous 45nm SOI technology node [1-2]. As CMOS technology progressed from planar devices to vertical structures such as the three-dimensional FinFET transistors, Grounded-Gate Gate-Non-Silicided ESD NFETs formed in the planar region are no longer an option and the fin-based MOSFET transistors show a much lower ESD performance due to the significant loss of silicon volume since the design is limited by the rules of fin pitch and gate spacing. To provide an ESD solution for mix-signal/high-voltage circuits in FinFET technology, a new alternative device named ESD lateral NPN (LNPN) is developed in 14nm FinFET SOI technology. During an ESD event, it can provide direct current conduction path from I/O pad to ground without relying on the low power bus resistance to

achieve adequate clamping voltage. Since the ESD devices using the planar-based approach show clear performance benefits over fin-based structures in terms of ESD failure current per device area [3], the LNPN devices in this study are all built in the planar region.

In this paper, we present comprehensive analysis of design and optimization of ESD LNPN device from two design approaches: Body-contact and Floating-body. The effects of key design factors such as base length, base doping, and body resistance on triggering and ESD performance of LNPN devices are investigated in detail using the two design approaches with the studies providing guidelines for the development of an optimized ESD lateral NPN device.

## II. Body-Contact Design

Figure 1 shows the cross section and top view of an SOI ESD LNPN device with a body-contact design. It consists of three terminals including the N+ emitter, N+ collector and P-body contact. The emitter and P-body terminals are tied together with metal wiring. Because of the thin SOI film thickness, the N+ and P+ diffusion can penetrate through the P- well region and reach the surface of Buried Oxide (BOX). This results in the butting emitter and collector junctions to form a lateral NPN structure (e.g., both base-emitter and base-collector junctions are formed in the lateral direction). The base length of the LNPN device is defined by the silicide-blocked region between the emitter and collector terminals. The P-body resistor (e.g., base resistance of NPN) needs to be formed in the third dimension since both N+ and P+ implantation touch the BOX layer.

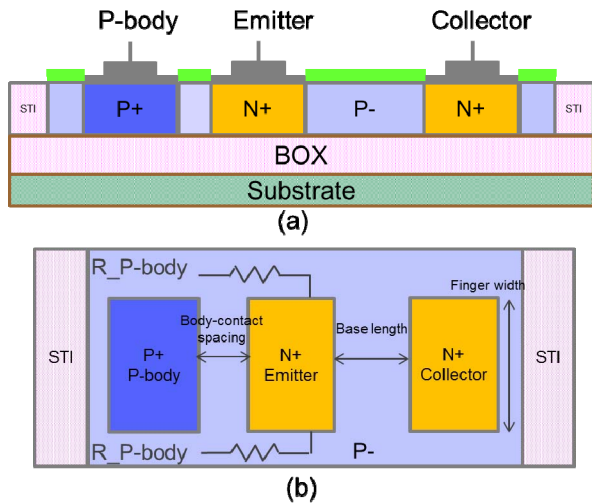


Figure 1: (a) cross-section and (b) top view of ESD SOI lateral NPN device with body-contact design

Figure 2 shows the 100ns TLP results of body-contact SOI LNP devices with width variation of 200 $\mu\text{m}$  and 300 $\mu\text{m}$ , all with a base length of 160nm and finger width of 5 $\mu\text{m}$ . The device width increases by increasing the total number of fingers. During the TLP measurement, the collector is stressed by pulses generated from the TLP system with a rise time of 10ns and pulse width of 100ns. The emitter and P-body terminals are grounded. The failure current is defined by the last data point in the TLP I-V curves before the DC leakage current shows five times or more leakage increase.

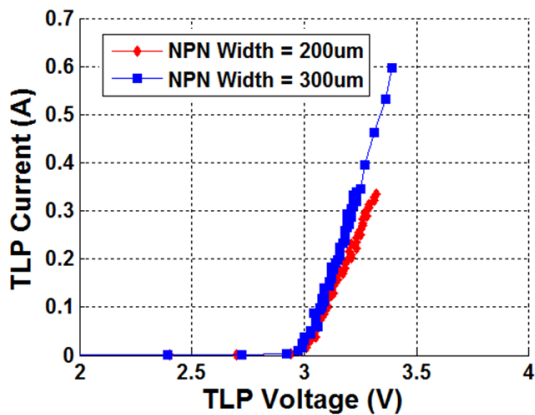


Figure 2: 100ns TLP I-V results of body-contact SOI LNP devices with width variation

As shown in Figure 2, both devices are able to turn on smoothly and sustain the current. There is no snapback behavior observed for the LNP devices. Compared to SCR-based solution having a low holding voltage after the snapback, the LNP device with non-snapback characteristic reduces the risk of latch-up issues for the application of high voltage ESD protection. The trigger voltage ( $V_{t1}$ ) of the

LNP device is  $\sim 2.9\text{V}$ . Good failure current scaling per width is observed with a normalized failure current of 1.5~2mA/ $\mu\text{m}$ . The ESD diode built in planar region can achieve a failure current of 5~6 mA/ $\mu\text{m}$  in the same technology. Considering the turn-on voltage of LNP is  $\sim 3\times$  higher than the diode and results in more heat dissipation under the same ESD current, the ESD performance of LNP device is comparable to that of the planar-based ESD diode in terms of the normalized power consumption per device area.

Two design parameters are investigated first to understand their effects on the ESD performance of body-contact LNP device: finger width and body-contact spacing. Figure 3 shows the 100ns TLP results of body-contact SOI LNP devices with finger width variation of 2.5 $\mu\text{m}$ , 5 $\mu\text{m}$  and 10 $\mu\text{m}$ . The definition of finger width is illustrated in Figure 1. All devices have a base length of 160nm and the same device width of 200 $\mu\text{m}$ . The LNP with smaller finger width has more number of fingers in the Y-direction so that the total width is constant. As shown in Figure 3, both trigger voltage and failure current of the LNP devices are affected by the finger width variation. A slightly increased trigger voltage and much reduced failure current are observed for the LNP with the smallest finger width of 2.5 $\mu\text{m}$ , which indicates possible multi-finger triggering issues due to the large number of fingers.

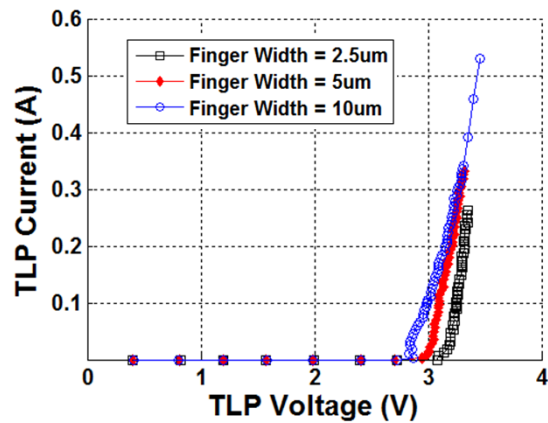


Figure 3: TLP I-V results of body-contact SOI LNP devices with finger width variation

Figure 4 shows the 100ns TLP results of SOI LNP devices with different body-contact spacing. The body-contact spacing is defined as the space between the P-body contact and N+ emitter terminal of LNP device. The larger body-contact spacing results in an increased bipolar base resistance. As show in Figure 4, the triggering of body-contact SOI LNP devices is not sensitive to the body-contact space due to their non-snapback characteristics. A slightly higher failure

current is observed for LNPNs with 2x and 4x body-contact spacing. However, the increased body space lowers devices' area efficiency and the 1x body contact spacing was determined to be the optimized design in terms of the highest failure current per unit area.

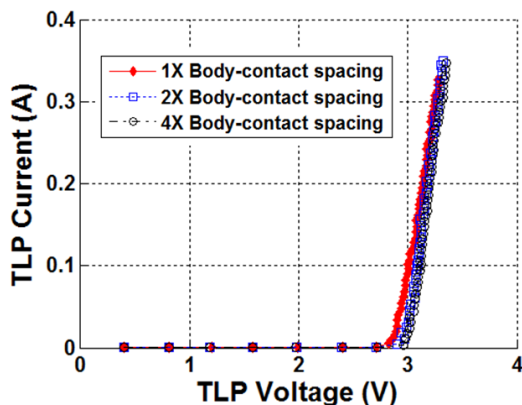


Figure 4: 100ns TLP I-V results of body-contact SOI LNPN devices with body-contact spacing variation

To achieve an effective ESD protection for high voltage applications, the trigger voltage needs to be designed properly. A lower trigger voltage will cause a higher DC leakage during normal circuit operation and a higher trigger/sustain voltage results in more power consumption and reduced ESD performance. The triggering of NPN device is sensitive to its bipolar characteristics including the current gain and base resistance. To design a proper trigger voltage, key design factors including NPN base length and base doping are studied to understand their effects to the bipolar characteristics and the triggering of LNPN devices.

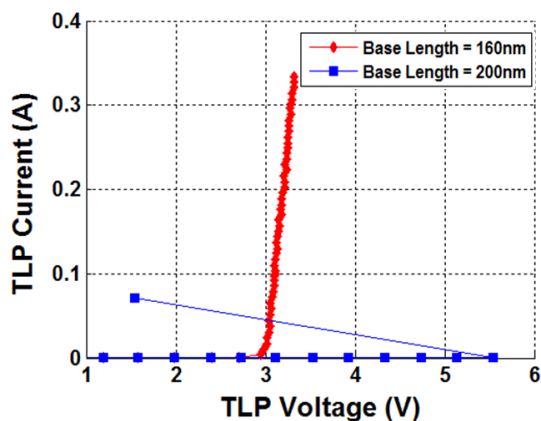


Figure 5: 100ns TLP I-V results of body-contact SOI LNPN devices with base length variation

Figure 5 shows the 100ns TLP results of body-contact SOI LNPN devices with base length variation of 160nm and 200nm, both device width of 200 $\mu$ m. As shown in Figure 5, with a small increase of 40nm in

base length, the LNPN device fails to trigger. This is because the larger base length results in a much reduced current gain and the NPN bipolar cannot generate enough base current to forward bias the base-emitter junction to turn on the device. On the other hand, a smaller base length may result in the punch-through. For LNPN device using the body-contact design, the triggering of the device is highly sensitive to the base length and a proper design of trigger voltage is hard to achieve by simply varying the base length.

Process optimization can be another approach to affect the LNPN triggering. Figure 6 shows the 100ns TLP results of body-contact SOI LNPN devices with process variations A, B and C as a function of P-well implant dosage. The P-well doping increases from process A to C. All the devices have a base length of 160nm and total width of 200 $\mu$ m. As shown in Figure 6, the LNPN devices with processes A and B have no problem to trigger and sustain the current. For LNPN with process B, with a higher P-well implant dose, the trigger voltage increases from 2.9V to 3.5V. A slightly reduced failure current is observed due to the higher holding/sustaining voltage after triggering causing more heat dissipation. The LNPN with process C, with further increased P-well dose, fails to trigger. Both bipolar gain and base resistance of the body-contact LNPN devices are strongly impacted by base doping. Higher P-well implant dose results in the reduced bipolar gain and base resistance. For the case of LNPN with process C, the base resistance is too low to produce enough voltage drops across the base-emitter junction to trigger the device. The proper design of LNPN triggering is still challenging in a narrow design window.

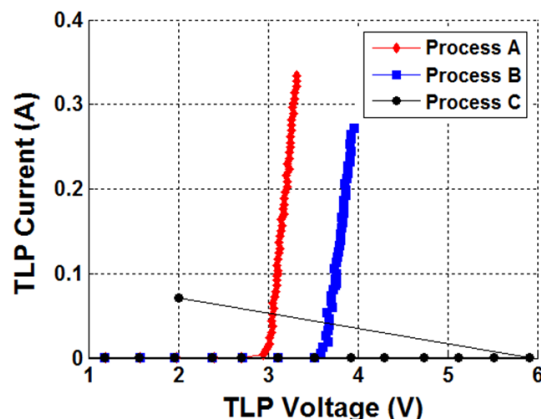


Figure 6: 100ns TLP I-V results of body-contact SOI LNPN devices with P-well implant dosage variation

The custom bipolar gain data under DC condition are also measured with the 3-terminal LNPN structures to understand their effects on the triggering of LNPN

devices. As shown in Figure 7, the bipolar gains are highly sensitive to the design of base length and base implant condition. For LNPN devices with base length of 160nm, the current gains drop significantly from process A to C with the increase of P-well implant dosage. A slower drop of bipolar gain is observed for the LNPNs with larger base length of 200nm. This is because the current gain is already low enough due to the increased bipolar base length. As shown in Figure 7, all the LNPN devices in the dash zone having much reduced current gain fail to trigger under the 100ns TLP measurements.

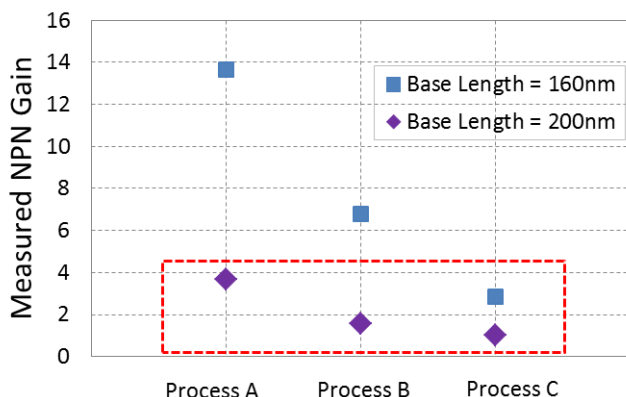


Figure 7: Measured NPN gain under DC condition with base length and P-well implant dosage variation

### III. Floating-Body Design

As discussed in previous section, the triggering of LNPN device with body-contact design is highly sensitive to its bipolar characteristics. A small increase of base length or base doping results in the significant decrease of bipolar gain and base resistance which can cause the LNPN device to fail at triggering. The enablement of a functional LNPN device is limited to a narrow design window in terms of process and dimension variation. To achieve more design flexibility, an alternative design using the floating-body approach is investigated in this section.

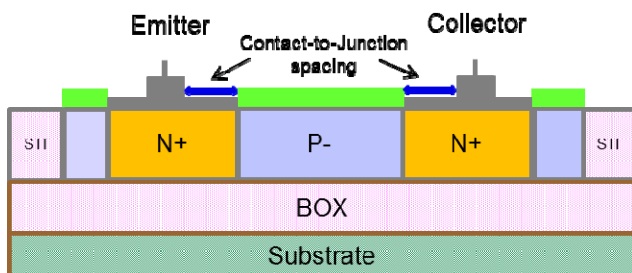


Figure 8: Cross-section of ESD SOI lateral NPN with floating-body design

Figure 8 shows the cross section of an SOI ESD LNPN device with floating-body design. It only consists of the N+ emitter and N+ collector terminals. The P- body contact is removed in the design to achieve the truly floated base region. All the other design dimensions are the same as the body-contact LNPN device. During the TLP measurement, the collector is stressed by the 100ns TLP pulses and the emitter is grounded. The symmetrical TLP I-V characteristics can be achieved with the TLP stress from the emitter to collector direction.

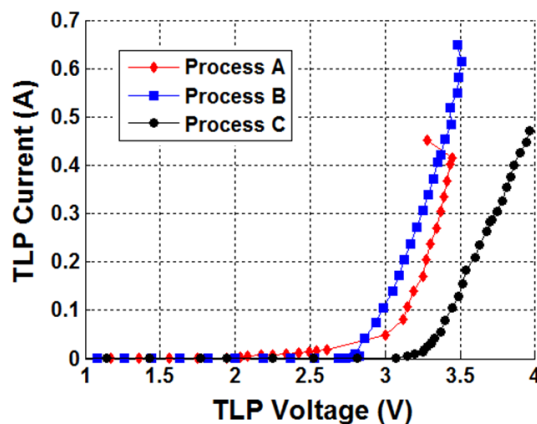


Figure 9: 100ns TLP I-V results of floating-body SOI LNPN devices with P-well implant dosage variation

Figure 9 shows the 100ns TLP results of floating-body SOI LNPN devices with the similar process variations A, B and C. As shown in Figure 9, compared to the body-contact design, the triggering of floating-body LNPN device is less sensitive to the base doping. All the devices, including the LNPN with process C (with highest P-well implant dose therefore the lowest bipolar gain and base resistance) have no problem in triggering and sustaining the current. This is because the base region is floating and the base resistance is no longer the gating factor in affecting the turn-on of LNPN device. The trigger voltage and ESD performance do show dependency on the base implant dosage. The LNPN with process A, having the lowest base doping, shows a significantly reduced trigger voltage. The LNPN with process C, having the highest base doping, turns on at the higher voltage due to the reduced bipolar gain. However, a lower failure current was observed since the higher holding/sustaining voltage after triggering results in more power consumption within the same silicon volume.

The DC measurements were also performed for the floating-body SOI LNPN devices with process variations A, B and C. The voltage bias is applied to the collector terminal and the emitter is grounded. As

shown in Figure 10, The LNPN with process A has a much reduced static breakdown voltage, however, the collector current increases gradually after the breakdown until the collector voltage reaches over  $\sim 3V$ . This is believed to be the cause of slow current increase of LNPN device with process A before its turn-on as shown in the TLP I-V of Figure 9. On the other hand, an abrupt current increase after breakdown is observed for both LNPN devices with process B and C and the DC breakdown voltage correlates well with the trigger voltage using 100ns TLP measurements. The LNPN with process C has the higher DC breakdown voltage but with a penalty of increased DC leakage current due to the higher P-well implant dose. Although the triggering of LNPN devices with floating-body design is less sensitive to the base doping, the process B is an optimum design to offer the best ESD performance and the lowest leakage current.

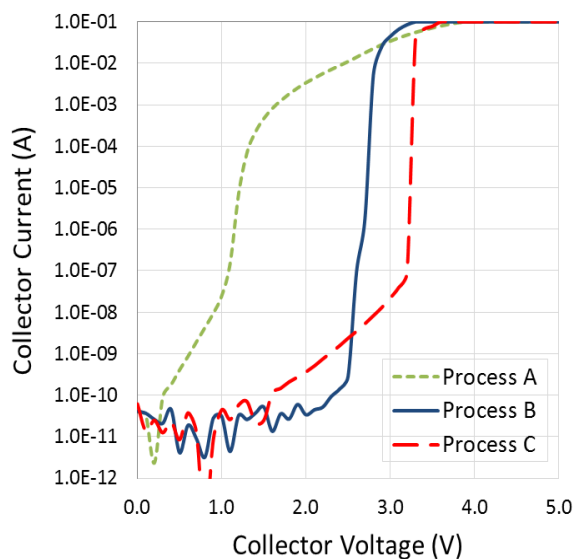


Figure 10: DC measurement results of floating-body SOI LNPN devices with P-well implant dosage variation

Figure 11 shows the 100ns TLP results of floating-body SOI LNPN devices with width varying from 200, 300 to 400 $\mu m$ , all with a base length of 160nm and base doping from process B. As shown in Figure 11, good failure current scaling per width is observed and a normalized failure current of 2.5~3mA/ $\mu m$  is achieved for the floating-body device. The floated body region gives clear performance benefits to the LNPN in terms of sustaining current. For the LNPN with body-contact design, the distributed base resistance is believed to be a factor in causing the non-uniform conduction along the device finger and results in a lower failure current for the same LNPN device width.

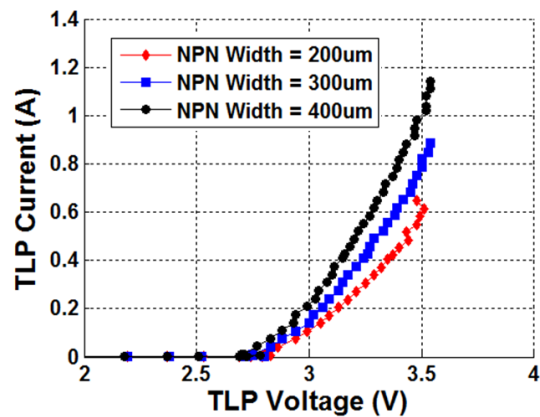


Figure 11: 100ns TLP I-V results of floating-body SOI LNPN devices with width variation

The capacitance of LNPN with body-contact and floating-body design is also measured at different device widths for comparison. As shown in Figure 12, the capacitance scales well with the LNPN width for both designs. The floating-body devices show a much lower capacitance compared to the body-contact design. This is because the base region is floating and the base-to-collector and base-to-emitter junction capacitors are connected in series and thus resulting in the reduced total capacitance. A capacitance of 0.56fF/ $\mu m$  is achieved for the LNPN device with floating-body design.

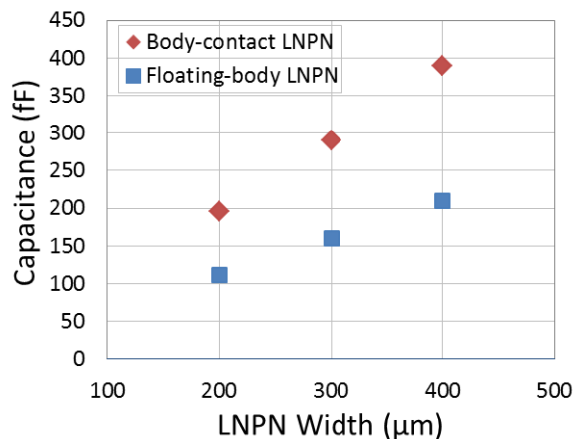


Figure 12: Measured capacitance of floating-body and body-contact SOI LNPN devices with width variation

However, as shown in Figure 11, the floating-body LNPN has a much reduced trigger voltage (e.g., 2.7V vs. 3.5V) compared to the body-contact device. To increase the trigger voltage, the effect of base length is re-evaluated for the floating-body design approach. Figure 13 shows the 100ns TLP results of floating-body SOI LNPN devices with base length variation of 160nm and 200nm, both having a device width of 200 $\mu m$  and a P-well implant dosage of process B. Unlike the body-contact design, no triggering issue is

observed for the floating-body LNPN device with the larger base length. Both devices are able to turn on smoothly and sustain the current. The trigger voltage increases from 2.7V to 3.1V with the base length increasing from 160nm to 200nm. A slightly reduced failure current is observed due to the higher trigger voltage. Compared to the body-contact device, the floating-body LNPN gives a higher flexibility to design the desired trigger voltage by varying the base length.

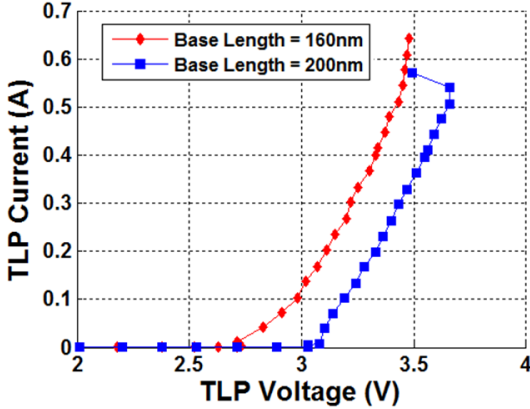


Figure 13: 100ns TLP I-V results of floating-body SOI LNPN devices with base length variation

To achieve a further improvement of ESD performance, the effect of another design factor named contact-to-junction spacing is studied. The definition of contact-to-junction spacing is illustrated in Figure 8. A larger contact-to-junction space results in the higher contact resistance at the collector and emitter regions. Figure 14 show the 100ns TLP results of SOI floating-body LNPN devices with contact-to-junction spacing varying from 170nm, 250nm, 330nm to 490nm. All the devices have the base length of 200nm and total width of 200 $\mu$ m. As shown in Figure 14, all the devices are able to trigger and sustain the current. The LNPN devices with the larger contact-to-junction spacing show a slightly higher on resistance but clear performance benefit in terms of the failure current since the heat generated at the contact is further away from the base. The normalized failure current increases to 3.5~4mA/ $\mu$ m for LNPN with contact-to-junction spacing of 490nm. However, the larger contact-to-junction space results in a penalty of increased on-resistance and device area. To offer a best overall ESD performance per device area, the contact-to-junction spacing of 250nm was determined to be the optimum design.

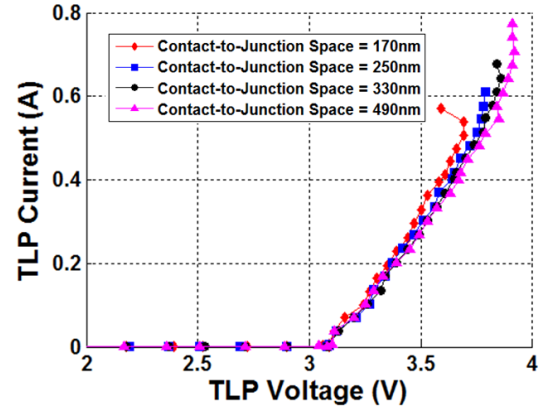


Figure 14: 100ns TLP I-V results of floating-body SOI LNPN devices with contact-to-junction spacing variation

VFTLP measurements with 1.2ns pulse width and 300ps on-wafer rise time were also performed. Figure 15 shows the VFTLP results of floating-body SOI LNPN devices with width varying from 200, 300 to 400 $\mu$ m, all with a base length of 200nm. As shown in Figure 15, all devices are able to turn on smoothly and sustain the current and the trigger voltage is slightly reduced under the fast transient due to the dV/dt effect [4]. Good failure current scaling per width is observed and a normalized failure current of ~12mA/ $\mu$ m is achieved under the VFTLP measurements.

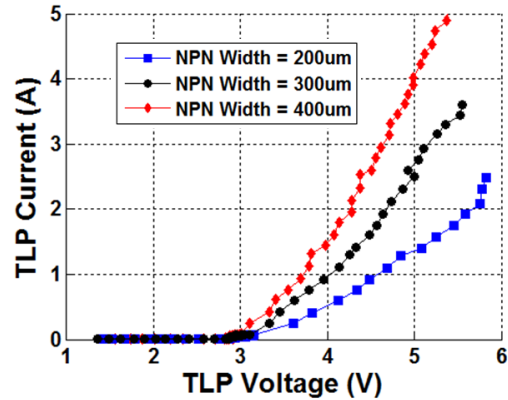


Figure 15: VFTLP results of floating-body SOI LNPN devices with width variation

## IV. Conclusion

We presented comprehensive analysis for development of SOI lateral NPN device by using body-contact and floating-body design approaches. The triggering of LNPN device with body-contact design is highly sensitive to its bipolar and distributed base resistance characteristics. A small change of base length and base doping can result in a significant decrease of bipolar gain and body resistance and cause the device fails to trigger. The body-contact LNPN device functions in a narrow design window with a failure current of 1.5~2 mA/ $\mu$ m. The triggering

and ESD performance of body-contact LNPN is insensitive to the body-contact spacing due to its non-snapback characteristics and an increased failure current and slightly decreased triggering voltage are observed for LNPN with larger finger width.

On the other hand, the triggering of LNPN device with floating-body design is less sensitive to the base doping. The higher failure current of 2.5~3mA/ $\mu\text{m}$  is achieved due to the floated body region. The trigger voltage can be properly designed by varying the NPN base length. A further improvement of failure current is achieved with larger contact-to-junction space. The device capacitance is also benefited from the floated body design and a capacitance 0.56fF/ $\mu\text{m}$  is achieved for the floating-body LNPN device.

Table1: Comparison of Diode, SCR and NPN-based ESD solutions for high-voltage I/O protection

	Ron ( $\Omega\text{-}\mu\text{m}$ )	Ifail per device width (mA/ $\mu\text{m}$ )	Ifail per device area (mA/ $\mu\text{m}^2$ )
Stacked diodes	236	5.5	2.4
Diodes in series with SCR	165	6.2	1.8
Lateral NPN	198	3	2.8

The ESD performances of the diode, SCR and LNPN based solutions for high voltage I/O protection are compared in Table 1. The normalized failure current per device width and area are extracted for each type of device. Although the LNPN device shows a lower failure current per device width, it stands out with highest failure current per layout area. Comparing to diode and SCR solutions, the LNPN device saves 15%~35% silicon area to achieve the same level of

ESD protection (e.g. 1kV HBM), corresponding to a decent on-wafer cost-reduction for the application of high voltage ESD protection.

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