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A Full-Chip ESD Protection Circuit Simulation and Fast Dynamic Checking Method Using SPICE and ESD Behavior Models

Feilong Zhang, Chenkun Wang, Fei Lu, Qi Chen, Cheng Li, X. Shawn Wang, Daguang Li and Albert Wang, *Fellow, IEEE*

***Abstract*— Full-chip electrostatic discharge (ESD) protection circuit design verification is needed for complex ICs at advanced technology nodes, which however is still largely impractical due to the limitation of ESD device models and CAD tools. This paper reports a new circuit-level ESD protection design simulation and dynamic checking method using SPICE and ESD device behavior models, which allows comprehensive, quantitative and dynamic verification of ESD protection circuit designs at chip level based entirely on ESD discharging functions. The new ESD protection circuit simulation method is validated using ICs designed and fabricated in a 28nm CMOS. This ESD-function-based ESD circuit simulation method is technology independent, which can handle various ICs including complex multiple power domain circuits and ICs using non-traditional ESD protection structures.**

***Index Terms*— ESD design method, circuit-level ESD simulation, behavior model, SPICE, I/O, RF switch.**

I. Introduction

As semiconductor technologies rapidly advance into nano nodes and FinFET technology domains, meanwhile IC chip complexity continuously increases, on-chip ESD protection design becomes extremely challenging. Circuit simulation can be conducted for simple timing analysis, which however cannot simulate ESD protection functions for most ICs that typically uses ESD protection structures featuring complex snapback I-V behaviors. Due to lack of accurate ESD device models and suitable full-chip ESD simulation CAD tools that can fully address the complex electro-thermal-process-device-circuit-layout coupling effects associated with ESD discharging behaviors, chip-scale ESD protection circuit design verification is still impractical for real world designs [1-8]. Over years, tremendous research efforts have been given to develop various ESD modeling and simulation techniques. TCAD-based mixed-mode ESD simulation-design method was reported to simulate small I/O blocks (circuit simulation) with ESD protection structures (numerical simulation) that do not require physics-based compact models for ESD devices [9, 10], which is however limited by the availability of process technology information and impractical to handle large circuits due to its numerical simulation nature. Physics-equation-based ESD device compact models were reported for ESD simulation [11-14], which however require full understanding of ESD device physics, often impossible, and extraction of too many device parameters. This makes using compact ESD device models very challenging and largely impractical for fabless designs that cannot ensure the model accuracy for arbitrary ESD devices and handle other simulation challenges, such as the convergence problem often seen in practical ESD circuit simulation [11, 15]. A new technology-independent ESD CAD tool was reported for whole-chip ESD protection circuit design verification [16, 17]. [16] discusses a novel CAD algorithm, featuring subgraph isomorphism and decomposition techniques, to extract arbitrary ESD structures and ESD-critical parameters of the extracted ESD devices. [17] presents a CAD flow that can generate an ESD netlist directly from an IC layout data file and then perform ESD-function-based design verification at chip level. While the ultimate goal was to allow ESD-function-based full-chip ESD protection circuit design verification, this ESD CAD method requires IC layout data and technology data, which may not be available to IC designers in fabless design houses [16, 17]. Alternative circuit and layout level ESD simulation techniques were also reported [18-22]. For example, [18] reports a chip-level dynamic ESD simulation technique. However, this simulation flow heavily relies on a numerical CAD method for substrate analysis, as well as technology and layout data, which are impractical for ordinary circuit designers. [19] describes using ESD sub-circuit models for ESD simulation by SPICE where ESD device models for simple diode and NMOS/PMOS ESD devices were discussed and validation using simple Zener ESD diodes and an RC-MOS power clamp was reported. This is a typical ESD simulation flow that has limited value in real-world ESD circuit simulation because of its limitation in availability, accuracy and scalability of ESD device models for arbitrary ESD structures due to the complexity of ESD discharging behaviors, such as high current and over-heating phenomena, layout irregularity and transient dV/dt effect. For example, the transient overshoot effect often observed in various ESD structures are very difficult to model

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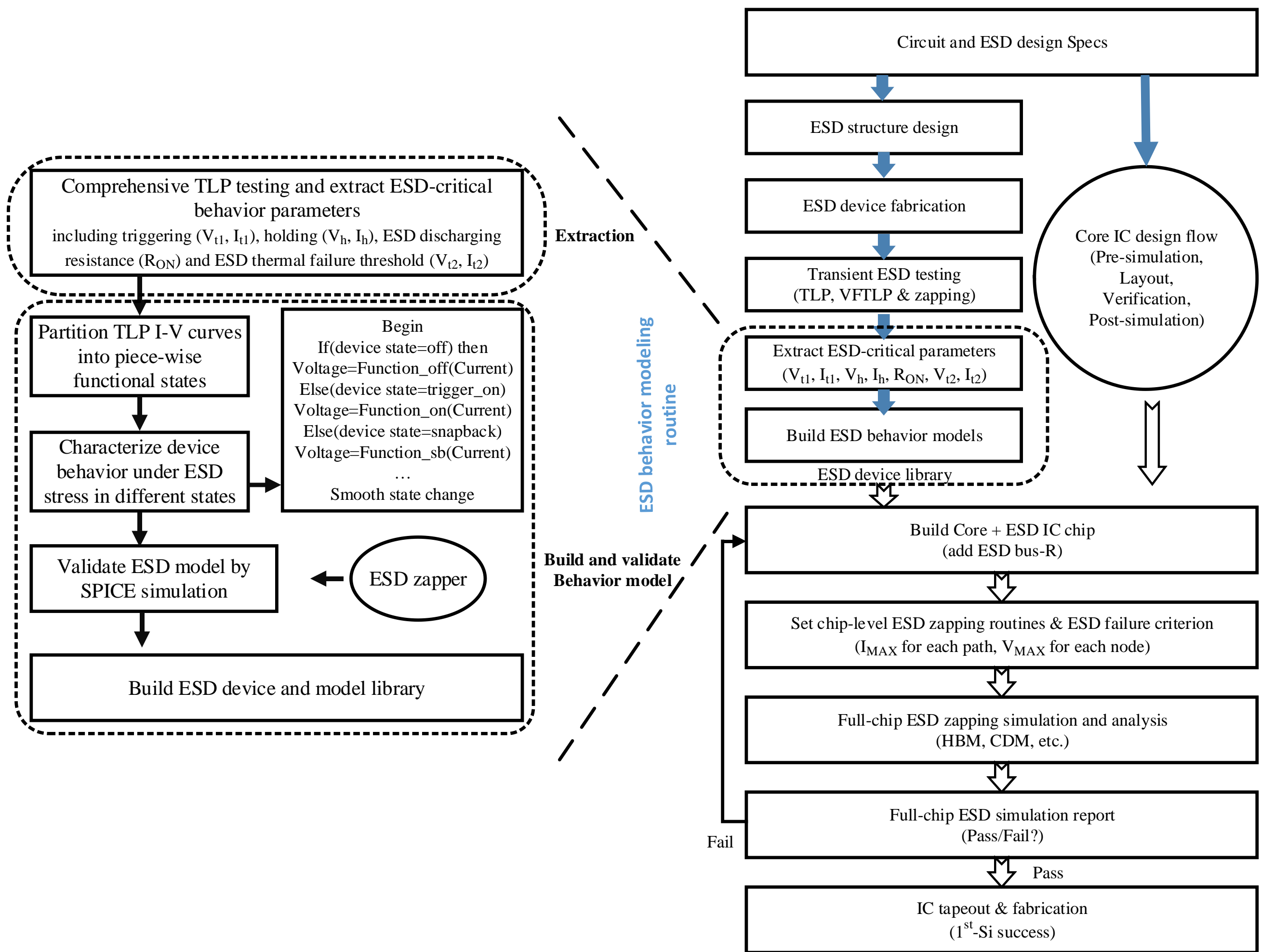

Fig. 1. A flow chart for the new full-chip circuit-level ESD protection circuit simulation and analysis method.

[20]. [21] depicts an integrated ESD checking flow focusing on DRC, topology and interconnect checking, which is a layout-centric static checking technique that cannot be used for transient ESD-function-based design verification. [22] presents a full-chip ESD simulation method, however, it can only check node voltage failures, ignored ESD current failures, and was only validated using simple ESD diodes. In summary, the reported ESD CAD methods still cannot allow ordinary IC designers to conduct quick transient and quantitative ESD circuit simulation without been limited by the availability of technology and layout data, and complexity, accuracy and scalability of physics-based ESD device compact models. In real-world IC designs, there is a strong and urgent demand for a practical circuit-level transient ESD simulation and quick dynamic ESD pass/fail checking technique, which shall allow ordinary IC designers to conduct comprehensive, quantitative and efficient full-chip ESD protection circuit simulation and design verification that is entirely based on ESD discharging functions. To address this need and based on a simple case study [23], this paper provides a comprehensive discussion of a new schematic-level ESD simulation and dynamic ESD checking method using SPICE and accurate ESD device behavior models, which was developed to enable ordinary IC designers to quickly and quantitatively verify ESD protection circuit designs at full chip level. This paper is organized as following: After the Introduction, Section II describes the general flow of the new circuit-level ESD protection design simulation method. Section III presents several practical design examples in 28nm CMOS and 45nm SOI to validate this new ESD simulation technique, followed by the Conclusion.

II. Circuit-Level ESD Protection Simulation

Circuit designers rely on CAD tools, e.g., SPICE, to design ICs following a common flow: schematic, pre-simulation, layout, post-simulation, verification, extraction, post-simulation and tape-out. The goal of this new circuit-level ESD protection circuit design method is to provide a SPICE-based circuit design flow allowing ordinary IC designers to conduct ESD-function-based full-chip ESD protection design simulation and analysis to verify ESD protection performance at full chip level before tape-out. Fig. 1 depicts the design flow of the new ESD circuit simulation method. The design flow starts from defining the specs for both core circuit and ESD protection of an IC chip. Typically, for a given IC technology, ESD structures will be designed and optimized, which will be fabricated and tested [4-10]. Comprehensive transient ESD characterization include transmission line pulse (TLP) for human body model (HBM), very-fast TLP (VFTLP) for charged device model (CDM) and ESD zapping test.

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TLP/VFTLP testing reveals all ESD-critical parameters, e.g., ESD triggering voltage (V_{t1}) and current (I_{t1}), holding voltage (V_h) and current (I_h), discharging resistance (R_{ON}), and failure voltage (V_{t2}) and current (I_{t2}) [1, 2], which define the ESD Design Window on a chip. Numerical characterization of an ESD protection structure or sub-circuit at chip level is required to accommodate the ESD Design Window Shrinking Effect for advanced IC technologies [24]. The transient discharging I-V characteristics for the ESD structures will be studied to extract the corresponding ESD device behavior models, with the brief modeling flow depicted in Fig. 1 [25, 26]. The advantage of ESD behavior modeling is that it circumvents the technical barrier of no good compact ESD device models for ESD circuit simulation. An ESD library will be built up consisting of the verified ESD protection structures and their behavior models for a given IC technology. This task is handled by either the IC foundries or the design service team in a fabless design house. Since the ESD behavior models are extracted from the measured ESD I-V curves, they are very accurate. An IC designer can go through the normal IC design flow to complete design of the IC core circuit. In the next step, the IC designer will select suitable ESD devices from the ESD library and integrated the selected ESD devices into the IC core to complete the whole IC chip (ESD + core circuit). It follows that the full chip (ESD + core) can be simulated using SPICE to study the ESD protection functions at circuit level. Since ESD current is typical very large, the metal bus resistance in an ESD discharging path may play a significant role in full-chip ESD protection design. Hence, the ESD interconnect resistance (bus-R) should be extracted and included in the chip-level ESD circuit simulation. At this point, circuit level ESD protection simulation can be conducted using SPICE similar to normal IC simulation except for: 1) using an ESD pulse as the stimulus, 2) following chip-level ESD zapping routines, and 3) analyzing ESD protection performance per ESD failure criteria. First, it is obvious that, for ESD circuit simulation, the input signals must be transient ESD pulses, i.e., the ESD pulse waveforms defined in ESD testing standards for HBM, CDM, MM, IEC or any other ESD testing models. The ESD stimuli can also be TLP or VFTLP waveforms. Second, unlike typical IC simulation using a small sinusoidal signal, chip-level ESD simulation routines are very complicated and time-consuming according to the industrial standard ESD zapping test procedures. Briefly, each pad (I/O, control and supply) must be zapped by a set of ESD pulses with respect to a reference pad, while all other pads on a chip have to be handled per an ESD testing standard selected, e.g., all open or all grounded. Meanwhile, each pad must be zapped against a positive supply pad (V_{DD}) and a negative supply pad (V_{SS}) positively (PD and PS modes) and negatively (ND and NS modes). Each supply pad (V_{DD}) must also be zapped against another supply pad (V_{SS}) positively (DS mode) and negatively (SD mode). Further, each pad must be zapped several times for each zapping mode, typically three times. Therefore, full-chip ESD zapping test is extremely tedious, time-consuming and costly, which makes the new chip-level ESD circuit simulation method even more desirable and valuable. Accordingly, a proper full-chip ESD zapping routine must be defined and programmed for ESD circuit simulation. Third, full-chip ESD simulation analysis is much more complicated than typical SPICE circuit simulation. According

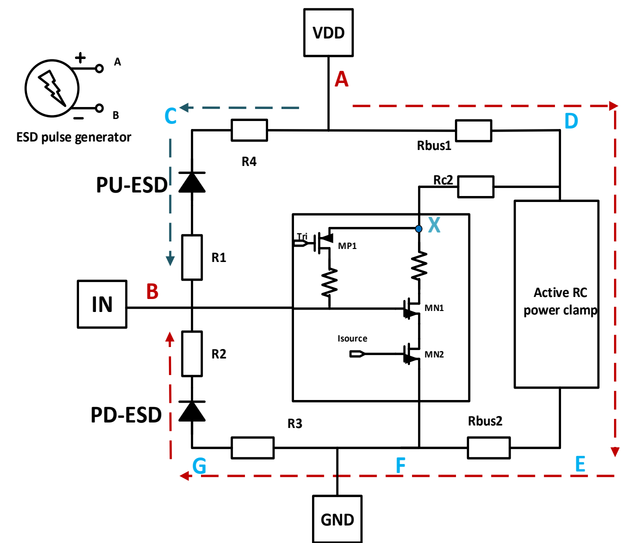

Fig. 2. Simplified functional diagram for the input buffer IC with full ESD protection for chip-level ESD protection circuit simulation. The key ESD metal resistances were extracted from its layout below.

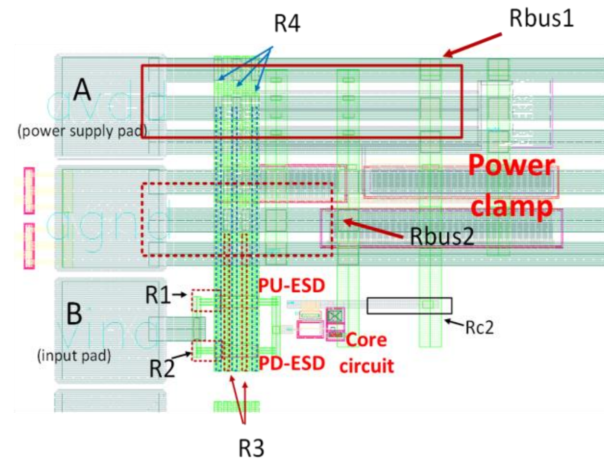

Fig. 3. Layout of the ESD-protected input buffer IC where key ESD metal resistances are extracted for full-chip ESD circuit simulation.

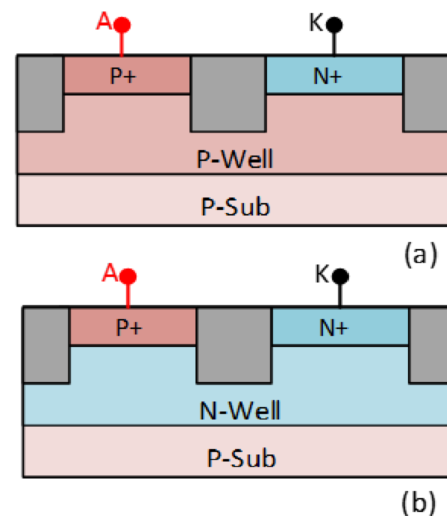

Fig. 4. Simplified cross-sections for the STI ESD diodes in this work: (a) N+/P-well PD-ESD diode and (b) P+/N-well PU-ESD diode.

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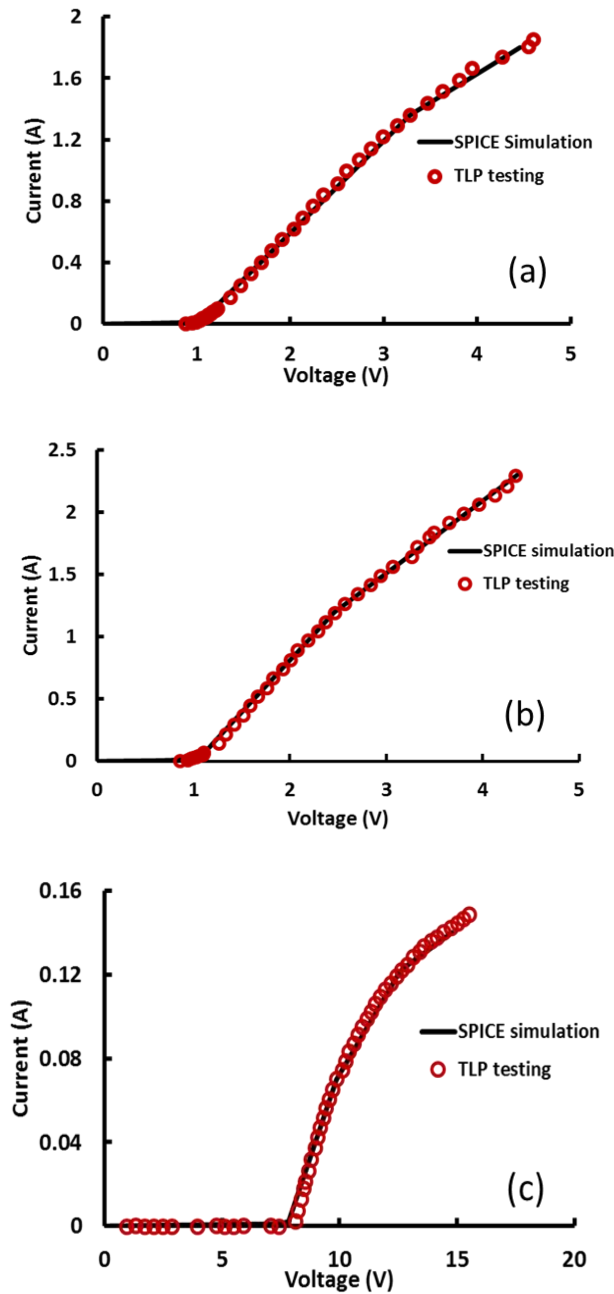

Fig. 5. Transient ESD I-V curves measured by TLP for, (a) N+/P-well diode (forward ESD mode), (b) P+/N-well diode (forward ESD mode) and (c) P+/N-well diode (reverse ESD mode), match well with SPICE simulation using the extracted ESD behavior models accordingly.

to the ESD-critical parameters and the ESD Design Window, chip-level ESD simulation must be analyzed for at least two ESD failure criteria: Criterion-1 is the maximum allowed voltage (V_{MAX}) at the protected nodes, typically defined by the breakdown voltage (BV) the nodes, against the simulated ESD clamping voltage (V_{ESD}) at the same nodes. If $V_{ESD}<V_{MAX}$ holds for all pads, then the chip passes the ESD testing; otherwise, ESD failure will occur. Criterion-2 is the maximum sustainable current (I_{MAX}) for each ESD discharging path against the simulated maximum ESD charging current (I_{ESD}) in the same path. Typically, I_{MAX} is same as the I_{t2} of the ESD protection structure. If $I_{ESD}<I_{MAX}$ holds for all ESD discharging paths, then the chip passes the ESD testing; otherwise, it fails the ESD testing. In practice, a safety margin (10%~20%) needs to be defined for an IC. The results for the whole-chip ESD circuit simulation should be analyzed carefully. If an ESD failure occurs, the IC designer will go back to check and revise the ESD protection designs, for example, using an ESD device featuring suitable V_{t1}, R_{ON} or I_{t2}. If the chip passes the comprehensive circuit-level ESD simulation, one can proceed to tape-out the design for fabrication and expect first-Si ESD design success. This new chip-level ESD protection circuit simulation and analysis method were validated by several ICs fabricated in foundry IC technologies as discussed below.

III. Design Validation and Discussions

The new circuit-level ESD simulation method was verified using several ICs designed and fabricated in foundry 28nm CMOS and 45nm SOI technologies.

A. *Input Buffer with Full ESD Protection*

The first example is an input buffer circuit with full ESD protection designed in a foundry 28nm CMOS. Fig. 2 shows the block diagram for the IC featuring ESD protection at the input and between the power supply buses with its layout shown in Fig. 3. The targeted ESD protection is 2KV per HBM model. The 28nm CMOS features V_{DD}=0.9V and typical breakdown of BV_{GS}=8.52V and BV_{DS}=7.01V, which defines the ESD Design Window. The input ESD protection utilizes an N+/P-well diode for power-down ESD protection (PD-ESD) against GND and a P+/N-well diode for power-up ESD protection (PU-ESD) against V_{DD}. Both ESD didoes, shown in Fig. 4, feature shallow trench isolation (STI) to minimize the parasitic capacitance for high-speed ICs. An active RC power clamp is used to protect the power rail. As part of the whole project, these ESD protection structures were first designed and fabricated, which were then characterized by TLP testing that delivers the transient ESD discharging I-V curves and their ESD-critical parameters, including the critical V_{t1}, V_h, R_{ON} and I_{t2}. Fig. 5

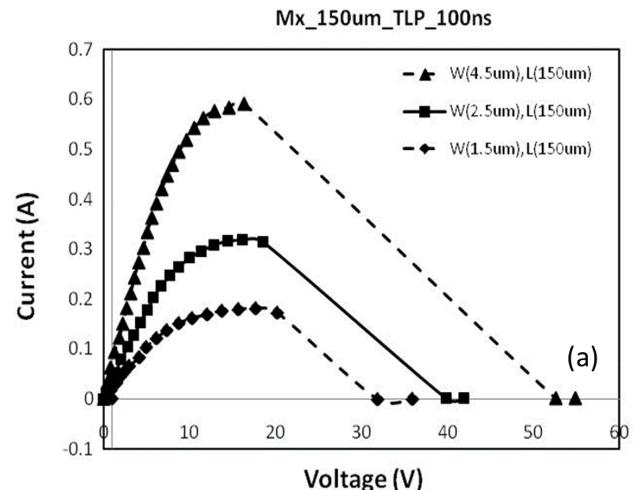

Fig. 6. Transient ESD I-V curves by TLP testing for an example M_X metal stack (M3-M7) used for ESD interconnects in this work.

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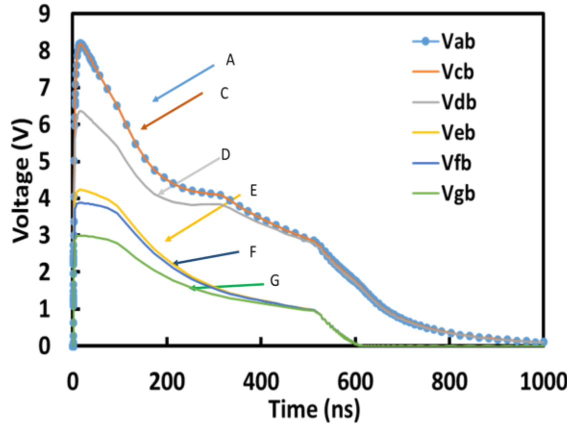

Fig. 7. Simulated transient node voltages for the ESD-protected input buffer IC using the new ESD simulation method under an ND mode 2KV HBM ESD zapping to the input pad (B) against V_{DD} (A). Note that all voltages are referred to node-B.

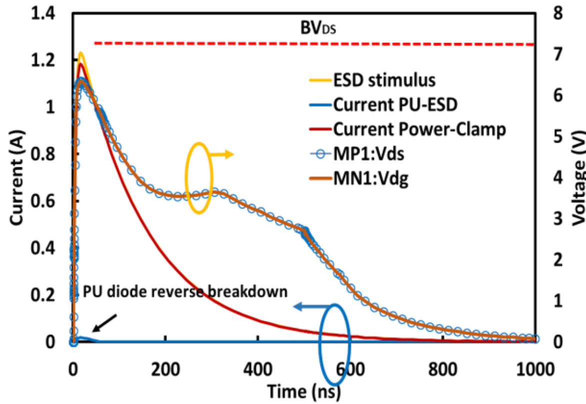

Fig. 8. Simulated branch currents (Left axis) and core circuit transistor voltages (Right axis) under the ND mode ESD zapping from Input pad (B) to V_{DD} (A).

presents the measured ESD discharging I-V curves for the ESD diodes that were used to extract the ESD device behavior models, which are saved in the ESD library for circuit-level ESD simulation. The TLP measurement shows that the ESD thermal failure currents are about I_{t2}=1.8A (i.e., HBM 2.7KV) for the PD-ESD diode and I_{t2}=2.3A (i.e., HBM 3.5KV) for the PU-ESD diode, respectively. The reverse ESD triggering voltage for the PU-ESD diode is about V_{t1}=-7.98V per TLP testing. Accuracy of the extracted ESD behavior models is critical for circuit simulation, which was confirmed by SPICE simulation for the ESD diodes using the corresponding ESD behavior models as depicted in Fig. 5. Due to large ESD currents, full-chip ESD circuit simulation must include key ESD metal interconnect resistances, which depends entirely on the IC layout. For this purpose, the metal interconnects for ESD connections are characterized first by TLP for the metal interconnects in the back-end-of-line (BEOL) of the 28nm CMOS. Fig. 6 depicts the transient I-V characteristics for one sample metal stack, the M_X (M2-M5), by TLP testing. The TLP-measured sheet-resistance is around $R_\square$=1Ω/☐ for M_X stack and $R_\square$=0.3Ω/☐ for the My stack (M8-M10), both used for ESD interconnects in this design. According to the layout (Fig. 3), the extracted ESD metal resistances are: R_{bus1}=1.5Ω between V_{DD} and power clamp anode (using M10, L=183µm and W=36µm), R_{bus2}=0.3Ω from the power clamp cathode to GND, R_1=1Ω between Input pad and cathode of PU-ESD, R_2=1Ω between Input and PD-ESD anode, R_3=1.15Ω from PD-ESD cathode to GND and R_4=0.6Ω from V_{DD} to PU-ESD anode. These key ESD metal bus resistors are included in schematic test bench as shown in Fig. 2. It is worth noting that, with the focus on ESD circuit simulation flow, we chose to use a simplified linear-fitting approach in estimating metal resistance. A more involving piece-wise linear curve fitting approach may be used to extract more accurate behavior models for ESD metal interconnects.

Comprehensive full-chip ESD circuit simulation using the new method was conducted for the ESD-protected input buffer IC to study its compliance against the ESD Design Window. The input stimuli for ESD simulation are 2KV HBM ESD pulses with the required ESD zapping routines and polarities as discussed previously. The simulated node voltages and branch currents under ESD stressing are carefully examined for the IC. Take one ESD zapping case as an example, which applies a negative HBM ESD pulse to the Input pad with respect to V_{DD} (i.e., ND ESD mode where the ESD pulse occurs to node B, while node A is grounded). Fig. 7 depicts the circuit node transient voltages under ESD zapping. Fig. 8 presents the ESD discharging currents and transient voltage for the core circuit transistors by ESD simulation. Per design, the intended main ESD discharging path would be the route-ADEFGB (Red line, conduction through the active ESD power clamp and PD-ESD diode in forward mode) that is confirmed by ESD circuit simulation (Figs. 2&8). Fig. 7 clearly shows that V_{DE}<2.5V for the power clamp, the voltage across the PD-ESD diode remains smaller than 2.7V, and the voltage from V_{DD} to GND across the core circuit (V_{DF}) is less than breakdown of BV_{DS} = 7.01V of the core circuit transistor, which confirms a successful design of the PD-ESD diode and the ESD power clamp. However,

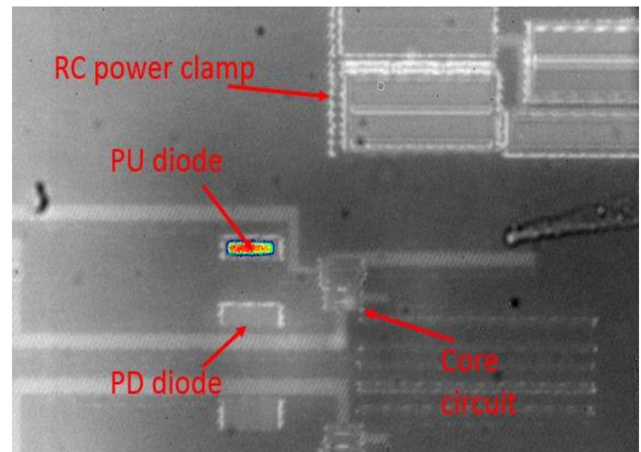

Fig. 9. An EMMI image under HBM zapping reveals a hot spot at the PU-ESD diode, indicating an ESD weak point in the design.

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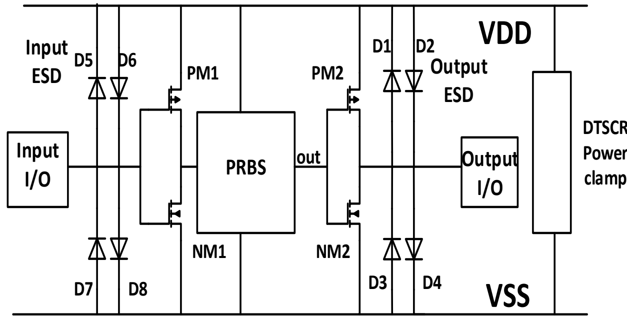

Fig. 10. A functional schematic for the ESD-protected PRBS IC where gated ESD diodes (D1-D8) protect I/O pins and the power clamp is a DTSCR.

ESD simulation also found a transient current of around 40mA in the route-ACB (Marked in Blue, conduction via PU-ESD diode in reverse mode, Figs. 2&8), which is because the voltage at Node-C exceeds the reverse BV (7.98V) of the PU-ESD diode (Fig. 7, i.e., the reverse ESD triggering voltage V_{t1}) during the ESD stressing period. Fig. 8 also confirms that V_{DS}<BV_{DS}~7.01V for MP1 and V_{GS}<BV_{GS}~8.52V for MN1 of the core circuit during the ESD stressing. This analysis suggests that the ESD design works for 2KV HBM zapping, though the PU-ESD diode (reverse mode) seems to be a weak point. This analysis was confirmed by the Emission microscopy (EMMI) image shown in Fig. 9 where a hot spot was observed at the PU-ESD diode location under HBM zapping. More analysis indicates that this issue may be associated with the higher-than-expected ESD metal resistance that led to a total voltage drop reaching to 4V, which may be revised by re-designing the ESD metal to reduce the total ESD discharging R_{ON}. In summary, this example validated the new chip-level ESD circuit simulation and analysis method and reveals its value of helping IC designers to analyze full-chip ESD design, to pin-down ESD design weak points and to optimize ESD protection design for a whole chip.

B. Large IC with Snapback DTSCR ESD Protection

The second example is a ESD-protected 7-bit pseudorandom binary sequence (PRBS) generator circuit, including D flip-flop and XOR gate, designed and fabricated in another foundry 28nm CMOS with BV_{DS}~5.6V and BV_{GS}~5.2V. The purpose is to validate the new ESD circuit simulation method using a large-scale IC with ESD protection featuring snapback I-V behavior that cannot normally be handled by SPICE simulation. Fig. 10 shows the IC schematic where I/O ESD protection devices are diodes and the power clamp is a diode-triggered silicon-controlled rectifier (DTSCR) ESD structure. An SCR

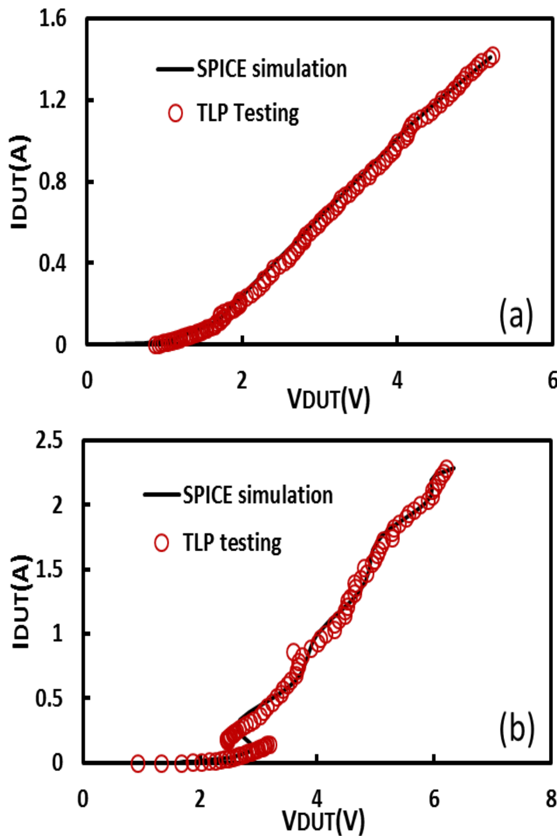

Fig. 11. ESD I-V curves by TLP testing (Red dots) agree well with SPICE simulation (Black line) using the extracted ESD behavior models for: (a) gated diode and (b) DTSCR.

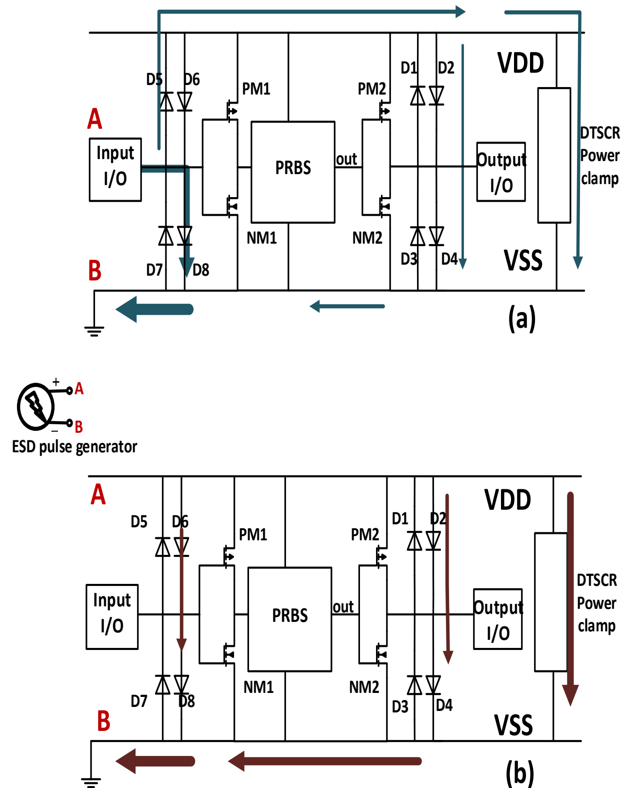

Fig. 12. Two exemplary full-chip ESD simulation cases: (a) positive Input-to-V_{SS} HBM zapping, and (b) positive V_{DD}-to-V_{SS} zapping. The arrowed lines indicate the possible ESD discharging paths with the thickness suggesting the amount of ESD discharging current.

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ESD protection structure is normally very ESD robust because of its snapback I-V behavior, low V_h, very high I_{t12} and very low R_{ON}. Unfortunately, the V_{t1} of SCR is too high for advanced CMOS. DTSCR utilizes diodes to trigger the SCR, hence achieves very low V_{t1}. Following the new ESD circuit simulation method, the diode and DTSCR ESD structures were designed, fabricated and characterized by TLP with the ESD I-V curves shown in Fig. 11. TLP testing found a very low V_{t1} ~ 3.19V for DTSCR, good for 28nm CMOS ICs, and V_{t1} ~ 1.03V at 10mA for the gated diodes, also suitable for I/O ESD protection in forward mode since V_{DD} = 0.9V in this 28nm CMOS. ESD behavior models were then extracted for the diode and DTSCR ESD devices, which were verified by SPICE simulation as shown in Fig. 11.

Comprehensive circuit-level ESD simulation was then conducted for the full chip by the new method using HBM ESD pulses as stimuli. Fig. 12 shows two exemplary ESD circuit simulation cases. First, Fig. 12a presents a positive Input-to-V_{SS} zapping case (PS mode) where D_8 is the intended ESD discharging path. In addition, two possible unintentional ESD

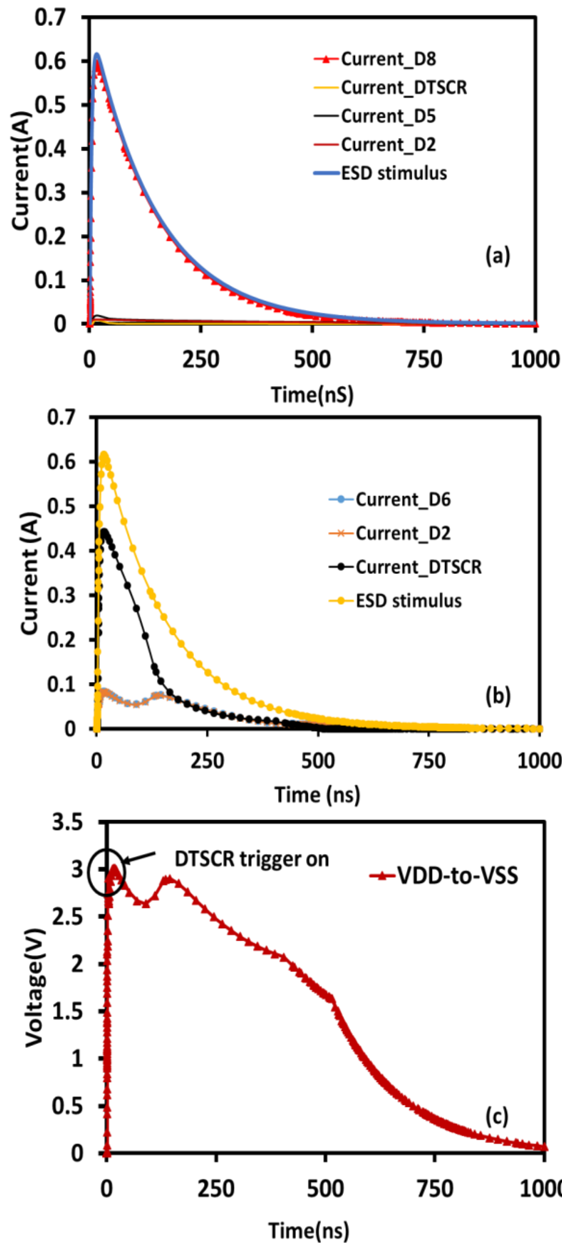
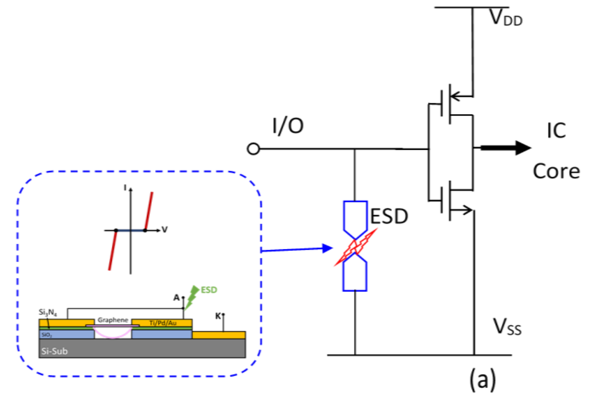


Fig. 13. Simulated transient ESD discharging behaviors for two ESD zapping cases of Fig. 12: (a) Input-to-V_{SS}, and (b) V_{DD}-to-V_{SS}.



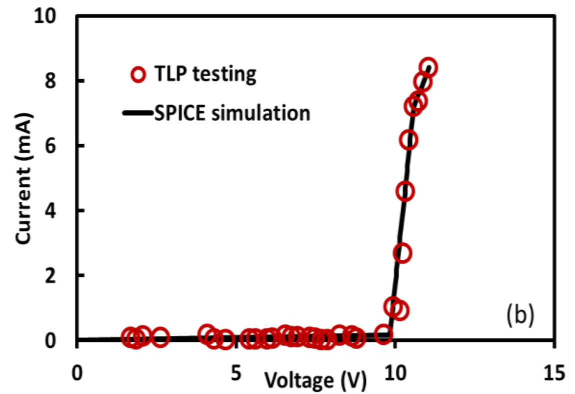


Fig. 14. A non-traditional above-Si gNEMS ESD protection structure: (a) gNEMS cross-section and ESD circuit scenario, and (b) ESD discharging I-V curves by TLP testing and SPICE simulation using its behavior device model match each other well. TLP testing shows V_{t1}~10V and I_{t2}~8.4mA for the gNEMS ESD device.

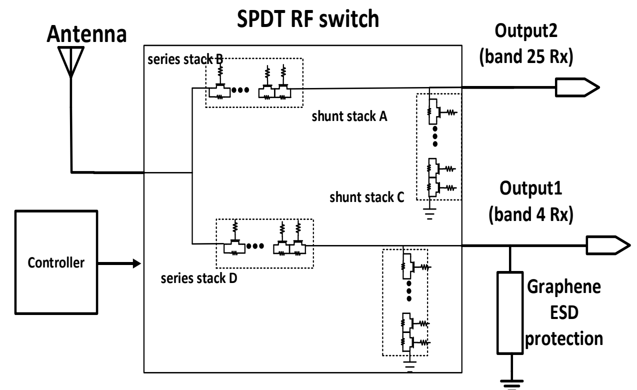


Fig. 15. A functional schematic of SPDT RF antenna switch circuit made in 45nm SOI CMOS with a gNEMS ESD protection fabricated by post-CMOS processing.

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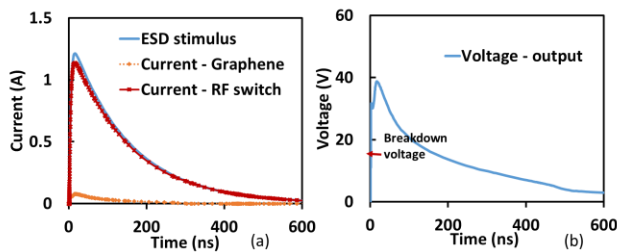

Fig. 16. (a) Simulated ESD current distribution for the SPDT circuit with gNMES ESD protection at the output pin. (b) Simulated output voltage for the ESD-protected SPDT circuit peaks at above 30V due to poor R_{ON} of gNMES ESD device.

discharging paths, D_5+DTSCR and $D_5+D_2+D_4$, may exist during HBM zapping. Fig. 13a depicts the simulated ESD discharging currents for each path, which readily shows that almost all ESD surge is discharged through input ESD diode (D_8) in forward mode as designed, while negligible current seen in any unwanted path. Fig. 12b depicts a positive V_{DD}-to-V_{SS} zapping case where the DTSCR power clamp is the intended ESD charging path, which is confirmed by ESD simulation given in Fig. 13b showing conducting >70% of the ESD stimulus due to very low R_{ON} in DTSCR. Meanwhile, there are two other unintentional paths, D_2+D_4 and D_6+D_8, which conduct a small amount of the ESD current as shown in Fig. 13b. The peak V_{DD}-to-V_{SS} voltage corresponds to the V_{t1} of DTSCR during HBM zapping. In summary, this design example confirms that the new ESD circuit simulation method can handle SCR-type ESD structures with snapback I-V behavior and works for large ICs for full-chip ESD circuit simulation and analysis.

C. RF Switch Circuit with Graphene NEMS ESD Structure

A good CAD tool should be technology-independent and be able to handle various emerging and non-traditional devices [26]. In fact, traditional in-Si PN-based ESD protection structures have many inherent disadvantages, such as parasitic capacitance, leakage and noise, which are becoming intolerable to parasitic-sensitive analog and RF ICs at nano nodes. Several novel non-traditional ESD protection structures were reported for future ICs at nano nodes [27-32]. For example, [27] reports an above-IC graphene-based NEMS (gNEMS) switch ESD structure, heterogeneously integrated into a CMOS back-end using a post-CMOS process. The third example is a single-pole-double-throw (SPDT) RF switch circuit designed and fabricated in a foundry 45nm SOI CMOS that is protected by the above-Si gNEMS ESD switch made by a post-CMOS process. Fig. 14a depicts the gNEMS ESD structure. The gNEMS ESD switch was fabricated in a post-CMOS process and characterized by TLP testing, as shown in Fig. 14b. The gNEMS ESD device remains OFF in normal IC operations. During an ESD event, the strong transient electrostatic force will pull down the suspended graphene membrane to touch the bottom electrode, hence quickly turns ON to discharge the ESD surge. The device behavior model was extracted for the gNEMS ESD device, which was verified by SPICE simulation using the extracted model as shown in Fig. 14b.

Fig. 15 shows a functional schematic for the SPDT circuit, designed as a LTE band switch between band4 and band25 with a maximum output power of +23dBm (V_{peak}=3.2V) and its output pin is protected by a gNEMS ESD device (V_{t1}~10V). SPDT uses a CMOS transistor stack to handle the output power that requires a total output-to-ground breakdown of BV~15V. Comprehensive circuit-level ESD simulation was conducted using the new ESD circuit method. Fig. 16(a) depicts the simulated ESD discharging current distribution among different circuit components, showing that most ESD current is discharged through the shunt transistor stack, because they are large and have self ESD protection capability. Fig. 16(b) shows that the transient node voltage peaks at above 30V, suggesting a potential ESD failure due to source-drain breakdown. While Fig. 14 shows that the individual gNEMS ESD device works nicely under TLP testing, Fig. 16 depicts that the gNEMS ESD device can only conduct small amount of the ESD surge at the chip level, which is attributed to its relatively large R_{ON} due to poor graphene contact. In summary, example-three shows that the new ESD circuit simulation method can handle non-traditional ESD protection structures as well, hence having a great potential for future ICs at nano nodes and featuring 3D heterogeneous integration.

IV. Conclusion

We report a new circuit-level ESD protection design simulation and dynamic analysis method using SPICE and ESD device behavior models. This new method allows ordinary IC designers to conduct fast, accurate and transient schematic-level ESD protection simulation without being limited by the availability and accuracy of IC technology information, layout data and physics-based ESD device compact models. The unique capability of the ESD-function-based circuit-level ESD protection transient simulation and dynamic ESD pass/fail checking technique makes it possible to verify whole-chip ESD circuit designs, therefore ensures first-silicon design success. The new ESD circuit simulation method was fully validated using three ESD-protected ICs designed and fabricated in foundry 28nm CMOS and 45nm SOI CMOS technologies.

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