Towards Optimal ESD Diodes in Next Generation Bulk FinFET and GAA NW Technology Nodes

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***Abstract*—**Beyond dimensional scaling, new process options in CMOS roadmap often result in degradation of ESD device performance. Using 3D TCAD and ESD characterization, the impacts of device architecture, middle-of-line contact scheme, and S/D epitaxy process options are explored on ESD diode performance in next generation bulk FF and GAA technologies.

I. Introduction

Bulk FinFET (FF) has become the mainstream technology in CMOS scaling roadmap. Bulk gate-all-around (GAA) vertically stacked horizontal nanowire (NW) has been proposed as a promising candidate in sub-7nm CMOS nodes [1-7]. ESD reliability has been investigated in bulk FF and bulk GAA stacked NW technologies [8-10]. A gate-defined diode (gated diode) and a STI-defined diode (STI diode) have been proposed and compared in these two advanced technologies [8, 10]. The STI diode has been demonstrated as the ESD protection diode with the higher failure current (*It2*) to parasitic capacitance ($C_{parasitic}$) ratio. The GAA NW STI diode even showed a better ESD performance, compared with the FF one. The reason has been explained by the difference of self-heating effect induced by different fin heights (H_{fin}) in these two technologies [10]. However, a related thermal heating during TLP (ESD) stress has not been presented in previous works. In addition, more process options including fin pitch (P_{fin}) scaling [7, 11, 12], wrap-around contact (WAC) scheme [7], and dual epitaxy processes for strain engineering [11-13], are proposed for next bulk FF and GAA NW technology nodes. They all have an impact on ESD diode performance. **The purpose of this work** is to study the impact of fin geometry scaling, middle-of-line (MOL) contact scheme change, and the corresponding S/D epitaxy process options on ESD diode characteristics in next bulk FF and GAA technologies. Self-heating during ESD stress has a strong impact on the diode's conduction and failure mechanism. This thermal behavior is explored by using 3D TCAD simulations.

II. ESD Diodes in FF and GAA NW Technologies

Fig. 1a shows a STI diode in FF and GAA stacked NW technologies. The STI diode architecture should be identical in these two technologies. However, the TLP *IV* characteristics of the STI diodes with 880 fins and 4 local interconnects (LIs) on the anode and cathode sides [10], **Fig. 1b**, present an on resistance (R_{on}) difference in these two STI diodes. Due to a different fin height (H_{fin}) in these two technologies, the diodes have different thermal behaviors, **Fig. 2** and **Fig. 3**. A taller fin structure usually has a large epitaxial volume on the anode and cathode regions. This improves the thermal dissipation and finally results in less self-heating in diode current conduction. **Fig. 3** shows that under a ~1A TLP stress current, which is used as a simulation reference current in this work, a difference of 150K in the simulated maximum lattice temperature (T_{max}) can be achieved. Not only the H_{fin} playing a key role, the STI depth (D_{STI}) impacts ESD diode performance because of the vertical current path through the fins in the STI diode [8]. **Fig. 4** shows significant influence (ΔT_{max} of 332K) on thermal heating by increasing D_{STI} from 40nm to 80nm, although the simulated R_{on} only increases 8% under the same TLP stress current. The T_{max} sensitivity to D_{STI} is higher, compared with the T_{max} sensitivity to H_{fin}, **Fig. 5**: a 32% T_{max} increases by increasing D_{STI} with 20nm, while a 24% T_{max} drop by increasing H_{fin} of 20nm. Fortunately, for CMOS scaling, H_{fin} will be increased for improving functional transistor performance, while D_{STI} will not. This is beneficial for ESD protection diode, as it will increase the corresponding *It2*. However, a taller fin architecture can result in a smaller contact area at the S/D regions due to the S/D epitaxy growth and the MOL process modules, which might impact failure levels, as illustrated in next section.

III. Impact of Geometry Scaling

With a H_{fin} of 50nm and a fin pitch (P_{fin}) of 45nm, the S/D epitaxy growth between two fins slightly touches each other. This allows an increased area of the contact scheme in MOL local interconnect (LI) processes, **Fig. 6a**. The contact scheme depth (D_{con}) is defined by the top of a Silicon (Si) epitaxy structure and the bottom of a LI recess ending depth in ILD0 layer. With a reduced P_{fin} of 30nm, the Si epitaxy structure between two fins will be merged. This results in a reduced contact depth (D'_{con}) in **Fig. 6b**. Taller fins with a further reduced P_{fin} will have more merged epitaxy volume. The contact scheme along the fin length has been shown to impact *It2* [8]. The reduced D_{con} can be expected to bring an impact on ESD diode performance, increasing its thermal heating under ESD and hence lower failure current. **Fig. 7** simulates the temperature distribution in the STI diodes with varying D_{con}. The T_{max} can increase 72% by reducing the D_{con} from 30 to 10nm, **Fig. 8**. Increasing D_{con} from 30nm to 50nm can reduce the T_{max} with 30%. A H_{fin} of 50nm with the D_{con} of 50nm allows a wrap-around contact (WAC) scheme [7].

However, the merged epitaxy structure not only causes a reduced D_{con} but also brings a reduced epitaxy volume. **Fig. 9** shows the impact of the epi-volume and D_{con} on thermal heating. With the same D_{con} of 20nm, but a 20% different epi-volume, **Figs. 9a** and **9b**, the thermal distribution did not show significant difference. The WAC scheme can reduce the thermal heating in the STI diode with the 20% reduced epi-volume, **Fig. 9c**. A detailed comparison of the impact of the epi-volume and D_{con} on lattice temperature (T_{max} and T_{ave}) is shown in **Fig. 10**. In general, D_{con} brings a more pronounced impact on T_{max}, compared with the epi-volume. For example, the T_{max} can be even reduced 22% in the STI diode with the WAC scheme but without any Si epitaxy structure (see **Fig. 10**). However, for providing the strain engineering in functional transistors, Si S/D epitaxy structure is replaced by SiGe S/D epitaxy structure [12, 13]. It is the first time that ESD results of FF and GAA NW diodes with the SiGe epitaxy structure are presented, as shown in next section.

IV. Impact of SiGe S/D Epitaxy Structure

Besides SiGe S/D epitaxy integrated in p-type MOSFETs, an in-situ doping process option has been proposed to replace the traditional ion implantation in heavy dopant diffusion (HDD) S/D regions due to a well-controlled doping profile [12, 13]. **Fig. 11** shows the TLP *IV* characteristics of STI diodes with a different epitaxy structure of Si or SiGe and a different doping process of HDD or in-situ Boron (B) dopant. A gated diode with the in-situ B doped SiGe epitaxy structure (SiGe:B) is also included for comparison. The *It2* and R_{on} have slight difference in the STI diodes with different epitaxy structures, because of a smaller SiGe epitaxy accompanying with a deeper D_{con} [12, 14]. However, the leakage monitoring results show a much higher leakage current in the SiGe:B epitaxy STI and gated diodes. The TLP *IV* characteristics of these diodes in a lower current region also show differences. First, the SiGe:B epitaxy gated and STI diodes have a lower V_{on} of 0.4V. Second, only the SiGe:B epitaxy STI one has a higher initial R_{on} just above V_{on} and then R_{on} reduced at 1.5V. The diode TLP *IV* looks like it has a "snapback" which is physically not possible in a normal diode. More accurate lower current DC measurements have been done in **Fig. 12**. Similar behaviors are observed, higher reverse leakage current and lower V_{on}, in the SiGe:B epitaxy gated and STI diodes together with the initial higher R_{on} in the STI one. These observations are only seen in the SiGe:B epitaxy p+/n-well diodes, but not seen in the ESD diodes with a n-type in-situ Phosphorus (P) doped in the Si epitaxy structure (Si:P). The Si:P epitaxy structure is used for S/D regions of NMOSFETs. The higher reverse leakage current, lower V_{on}, and even the initial higher R_{on} in the diodes with the SiGe:B epitaxy are linked to the SiGe/Si heterostructure interface.

A simplified device simulation setup built and the results are shown in **Fig. 13**. Three different scenarios of the offset between the locations of SiGe/Si heterostructure interface and p+/n-well junction are compared. They are: 1) a zero-offset ("0"), 2) a negative offset ("-") which means a p-type dopant out diffusion from the SiGe/Si heterostructure interface, and 3) a positive offset ("+") which represents the p-type dopant depletion at the bottom of SiGe epitaxy structure in **Fig. 13**. The corresponding band diagrams of these three offset scenarios are shown in **Fig. 14**. The simulated *IV* results, **Fig. 13,** show that the STI diodes with the "0" and "+" offsets have a much higher R_{on} compared with the ones with the "-" offset. The R_{on} is reduced by increasing the "-" offset values and approaches the R_{on} of a pure Si reference diode without SiGe/Si heterostructure interface. The inserted figure of **Fig. 13** shows that the low current V_{on} is influenced by the offset between heterostructure and junction interfaces. The V_{on} of the diode with the "-" offset is similar to the V_{on} of the Si reference diode. The V_{on} for "0" and "+" offset are in between of the V_{on} values of a SiGe reference diode and the Si reference diode, both without heterostructure interface.

The root cause of the higher initial R_{on} in the "0" and "+" offsets, **Fig. 13** and **Fig. 14**, is related to the impact of the valance band offset, $\Delta E_{V,\,offset}$, at SiGe/Si heterostructure interface for the different offset values. The $\Delta E_{V,\,offset}$ in the "0" and "+" offsets induce a significant energy barrier for the hole (h+) carrier transport from p+ region to n-well under forward-biased condition. The high reverse leakage current and lower V_{on} in these two offsets can be attributed to a lower energy barrier of electrons (e-) at the p+/n-well junction interface, **Fig. 14**. On the other hand, the $\Delta E_{V,\,offset}$ reduction in the "-" offset results in a much lower R_{on}. A higher junction barrier causes a higher V_{on} and lower reverse leakage current in the "-" offset. In **Figs. 11** and **12**, the difference between the SiGe:B epitaxy gated and STI diodes in the TLP and DC *IV* characteristics can be also well explained by the different impacts between the "0" (or "+") and the "-" offsets. The gated diode has two different offset scenarios at different junction locations. First, with an p-type extension implant under the sidewall spacer of a dummy gate structure, the surface current path, which is a dominant current path in the gated diode [8], will become the "-" offset scenario. This can be a main reason of lower initial R_{on} in the gated diode. The higher reverse leakage current and lower V_{on} also shown in the gated diode can be attributed to the bottom junction under the anode p+ SiGe:B epitaxy structure. This is similar to the SiGe:B epitaxy STI diode with the "0" (or "+") offset scenario.

TLP measurements on a simple planar diode with Ge/Si heterostructure interface confirm the model. It shows the similar impacts of the lower V_{on} and the higher R_{on} below ~1.5V, **Fig. 15**. In addition, the SiGe:B epitaxy STI diodes with 50% or 70% Ge content and varied in-situ B concentrations show very similar impacts in the measurements and simulations. However, the n-type doping concentration in n-well plays a dominant factor for this heterostructure interface effect in the SiGe:B epitaxy STI diodes. **Fig. 16** shows the R_{on} can significantly reduce by increasing n-type doping concentration, such as the ground plane (GP) implants in the GAA NW technology [6, 10]. With a higher doped n-type region ($5e18cm^{-3}$), the R_{on} can be drastically drop because of a smaller depletion region in n-well and a possible tunneling of carriers between p+ SiGe valance band, $E_{V,\,SiGe}$, and n-Si conduction band, $E_{c,\,Si}$. The effective "-" offset value for preventing the unwilling hetero-interface effect of the higher R_{on} and higher reverse leakage in the SiGe:B epitaxy STI diodes will strongly depend on the n-type Si doping concentration, **Fig. 17**. However, the parasitic capacitance ($C_{parasitic}$) which is an essential ESD design parameter will be significantly increased by high n-type doping concentration [10]. Finally, to increase the "-" offset value can be done by a top-up HDD implant, which might be an easy solution for ESD diodes because of no DIBL concern in ESD diodes. **Fig. 18** shows the SiGe:B epitaxy gated and STI diodes with an additional top-up p-type HDD implant. A lower reverse leakage current and no higher initial R_{on} in DC and TLP measurement results are observed.

V. Conclusion

ESD diodes in sub-7nm FF/GAA are significantly impacted by the process options of fin geometry, S/D epitaxy and MOL manufacturing modules. The contact depth (D_{con}) of LI access area on S/D epitaxy structure is one of the most important factors in these process options. A wrap-around contact (WAC) scheme is a most beneficial process option for ESD protection diodes. The process option of an in-situ B doped SiGe epitaxy structure results in several negative impacts on ESD diode performance. An optimized junction depth in the SiGe:B ESD diode is the most essential process parameter for preventing the problem induced from the SiGe/Si heterostructure interface. A top-up HDD implant optimizing the junction depth can be an attractive solution to prevent the heterostructure interface impact.

References

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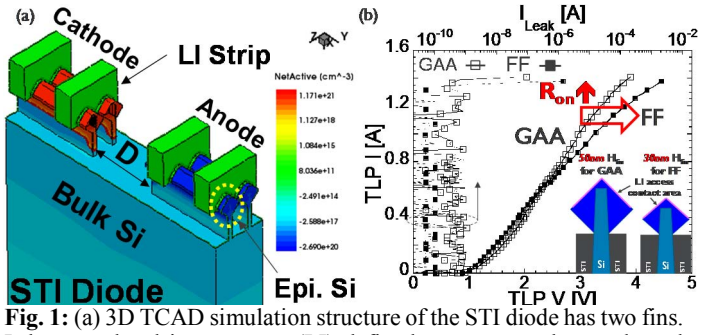


Fig. 1: (a) 3D TCAD simulation structure of the STI diode has two fins. It has two local interconnect (LI) defined contacts on the anode and cathode sides. The anode to cathode spacing (D) in the STI diode is 140nm. (b) In Ref. [10], the measured TLP *IV* of the STI diodes in the different processed wafers of FinFET and GAA NW with a fin height (H_{fin}) of 30nm and 50nm, respectively.

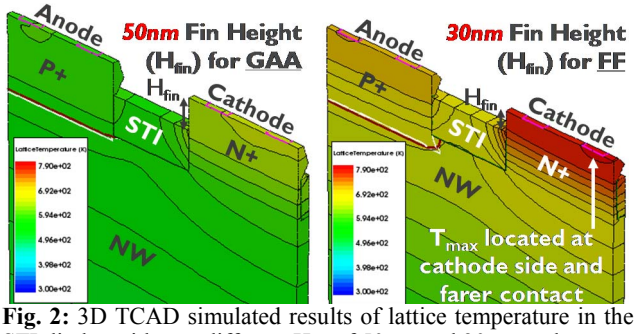


Fig. 2: 3D TCAD simulated results of lattice temperature in the STI diodes with two different H_{fin} of 50nm and 30nm under same TLP stress condition. A half fin architecture is used for the 3D TCAD device simulations. The 3D views are at the middle of a unit fin. The STI diodes have LI numbers (N_{LI}) of 2 on the anode and cathode sides and the anode to cathode spacing (D) of 140nm.

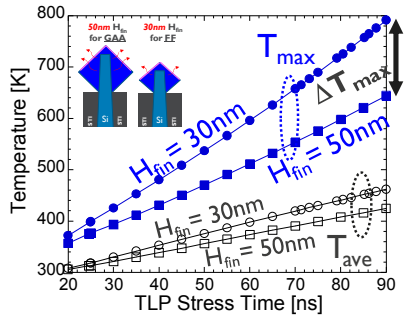


Fig. 3: Simulated results of corresponding maximum and average lattice temperature (T_{max}: solid symbols and T_{ave}: open symbols) values during a stress window between 20ns and 90ns in Fig. 2.

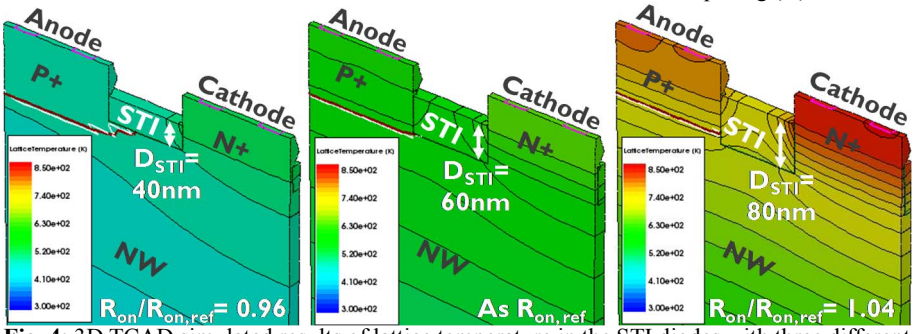


Fig. 4: 3D TCAD simulated results of lattice temperature in the STI diodes with three different STI depth (D_{STI}) of 40nm, 60nm and 80nm under same TLP stress condition. The STI diodes have same N_{LI} of 2 on the anode and cathode sides, the D of 140nm, and the fixed fin height (H_{fin}) of 50nm. The corresponding R_{on} to $R_{on,\,ref}$ ratio in the STI diodes with D_{STI} of 40nm, 60nm and 80nm are shown at bottom of each figure.

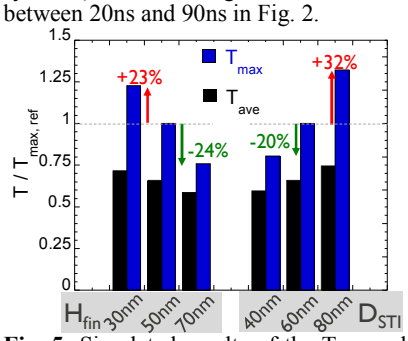
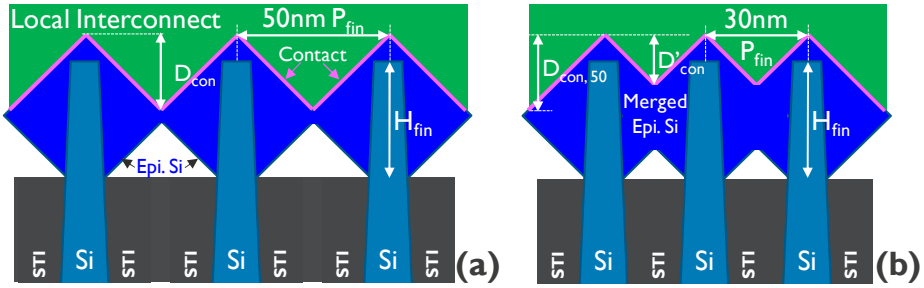


Fig. 5: Simulated results of the T_{max} and T_{ave} ratio in the STI diodes with three different H_{fin} and D_{STI}. The T_{max} of the STI diode with the D_{STI} of 60nm and the H_{fin} of 50nm is the reference ($T_{max,\,ref}$).



H_{fin}= 50nm and P_{fin}= 45nm **H_{fin}= 50nm and P_{fin}= 30nm**

Fig. 6: Schematic cross-sectional views at the anode (or the cathode) side of the STI diodes with a fixed H_{fin} of 50nm but two different fin pitches (P_{fin}) of (a) 45nm and (b) 30nm. (b) Due to a further merged epitaxy structure, the contact depth (D_{con}) is reduced to a shallower contact depth (D'_{con}) between two fins in the STI diode with the P_{fin} of 30nm.

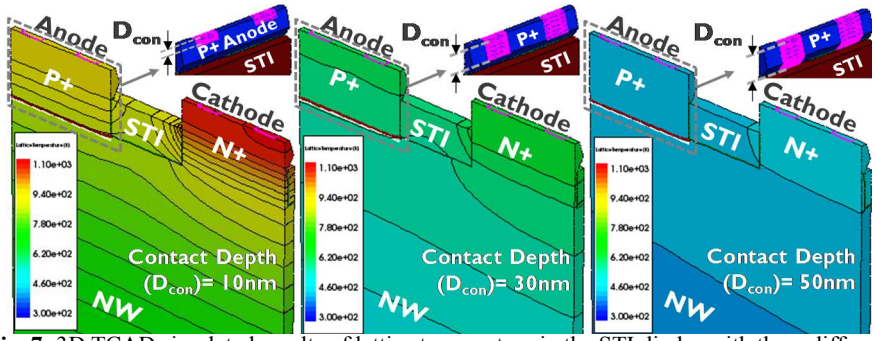


Fig. 7: 3D TCAD simulated results of lattice temperature in the STI diodes with three different contact depth (D_{con}) of 10nm, 30nm and 50nm under same TLP stress condition. When the H_{fin} is equal to the D_{con}, this is a wrap-around contact (WAC) scheme. The STI diodes have the N_{LI} of 2 on the anode and cathode sides, the D of 140nm, the H_{fin} of 50nm, and the D_{STI} of 60nm. In addition, the epitaxy structures are also fixed in these three STI diodes.

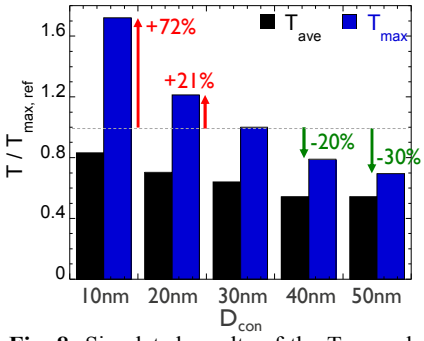


Fig. 8: Simulated results of the T_{max} and T_{ave} ratio in the STI diodes with five different D_{con} from 10nm to 50nm. The T_{max} of the STI diode with the D_{con} of 30nm is the reference ($T_{max,\,ref}$).

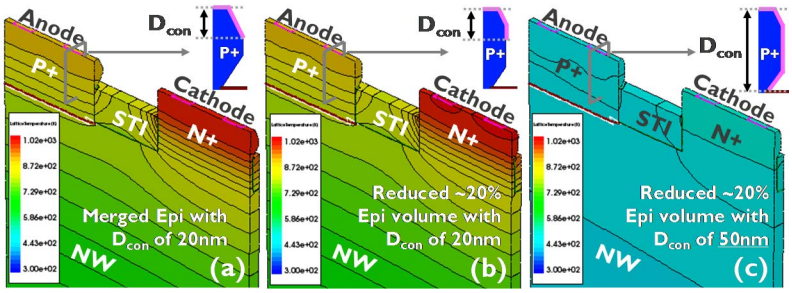


Fig. 9: 3D TCAD simulated results of lattice temperature in the STI diodes with (a) and (b) two different epitaxy volumes, and with two different corresponding contact depths (D_{con}) of (b) 20nm and (c) 50nm under the same TLP stress level. With the H_{fin} and D_{con} of 50nm, (c) is the wrap-around contact (WAC) scheme. The STI diodes have same N_{LI} of 2 on the anode and cathode, the D of 140nm, the H_{fin} of 50nm, and the D_{STI} of 60nm.

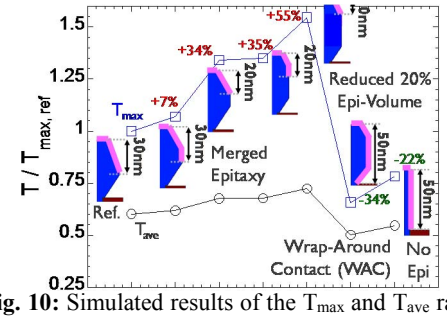
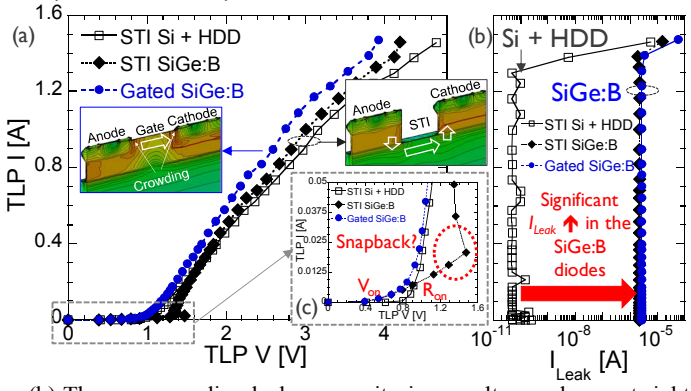


Fig. 10: Simulated results of the T_{max} and T_{ave} ratio in the STI diodes with different epitaxy volume and corresponding D_{con}. The T_{max} of the STI diode with non-merged epitaxy shape and D_{con} of 30nm is the reference ($T_{max, ref}$).

Fig. 11: (a) Measured TLP *IV* curves of the gated and the STI diodes in the different processed wafers. These two wafers have very different process options in p-type S/D epitaxy and dopant module. One is Si epitaxy with standard p+ HDD implant. The other one is SiGe epitaxy with an in-situ Boron (SiGe:B) doping process. (b) The corresponding leakage monitoring results are shown at right. (c) The mid-bottom small inserted figure is the zoom-in view of the measured TLP *IV* curves.



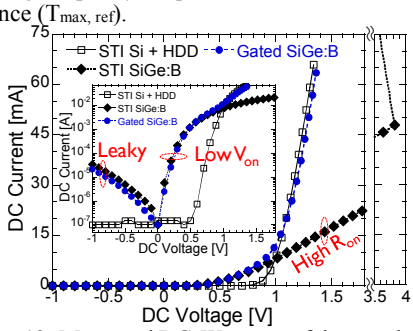


Fig. 12: Measured DC *IV* curves of the gated and the STI diodes with different epitaxy materials and different p+ doping processes. Inserted figure is the same measured DC *IV* curves with the y-axis of current in log scale.

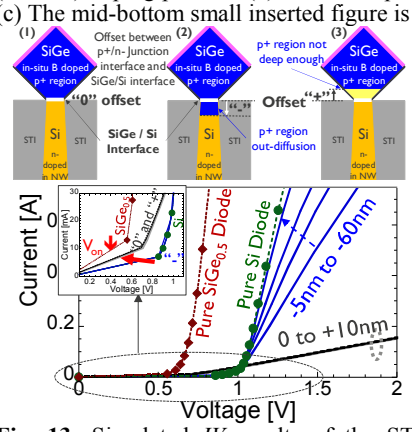


Fig. 13: Simulated *IV* results of the STI diodes with different offset scenarios of the locations between SiGe/Si heterostructure interface and p+/n-well junction interface.

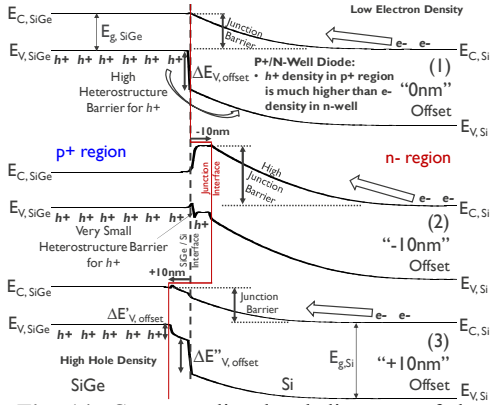


Fig. 14: Corresponding band diagrams of the three different scenarios of the offsets of (1) 0nm, (2) "-"10nm, and (3) "+"10nm between junction interface and SiGe/Si interface.

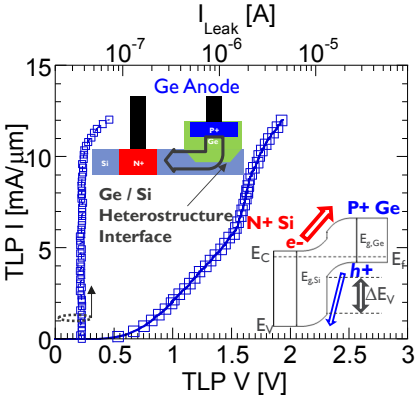


Fig. 15: Measured TLP *IV* curves of a SOI planar Ge/Si heterostructure diode. Inserted figure is the corresponding band diagram of Ge/Si interface.

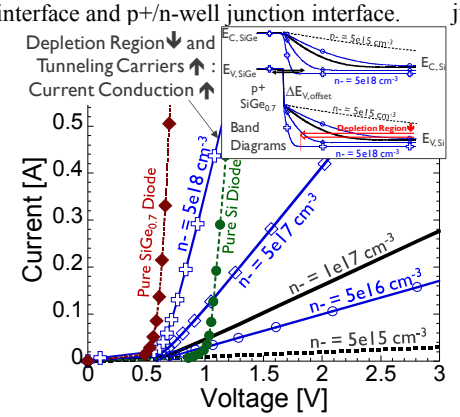


Fig. 16: Simulated *IV* results of the STI diodes with varied n-well doping concentrations but a fixed offset of 0nm between the SiGe/Si interface and p/n junction interface.

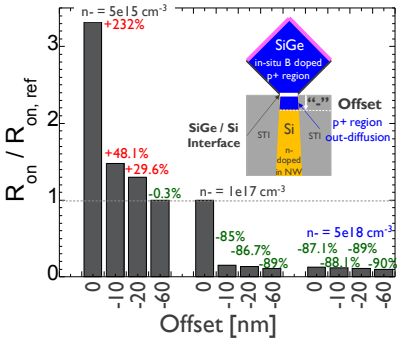


Fig. 17: Simulated results of the R_{on} ratio in the SiGe/Si STI diodes with three varied n-well doping levels from 5e15 to 5e18 cm^{-3} and four varied offset values. The reference one is 1e17 cm^{-3} and 0nm offset.

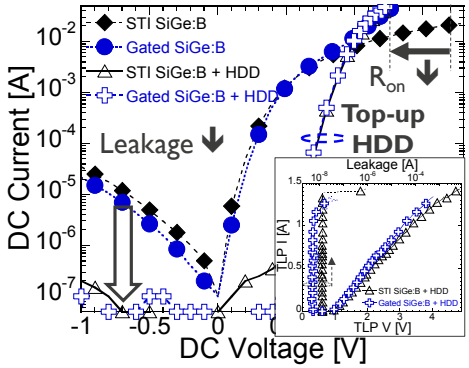


Fig. 18: Measured DC *IV* curves of the gated and the STI diodes with same epitaxy materials but two p+ doping processes with and without top-up HDD implant. Inserted figure is the measured TLP *IV* curves.