A Compact and Self-Isolated Dual-directional Silicon Controlled Rectifier(SCR) for ESD Applications

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Abstract—In this paper, a compact and self-isolated dual directional silicon-controlled rectifier (CSDDSCR) developed in a single N-well has been proposed and demonstrated. Without using the P-well, N-type isolation structure as well as an auxiliary trigger component which are normally required in the traditional DDSCR, the novel CSDDSCR possesses a very high area-efficiency and robustness of ~8.81V/μm^2. It is also shown that the CSDDSCR preserves a lower trigger voltage as 10V, an adjustable holding voltage from 3.32V to 8.79V under the TLP test, a smaller overshoot voltage of ~19V at 2A VFTLP stress as well as an extremely low leakage current of ~94pA measured at 3.3V, making it a superior candidate for ESD protection in the 3.3v/5v CMOS processes. Moreover, a holding voltage reversal (HVR) effect has also been discovered and explained with TCAD simulation.

Index Terms—Area-efficiency, dual-directional SCR(ddSCR), electrostatic discharge(ESD), holding voltage reversal effect.

I. Introduction

The growing popularity of portable and wearable consumer electronics impose a strong demand for effective and robust electrostatic discharge (ESD) protection solutions [1]. However, traditional ESD protection cells usually consume a larger chip area and increase the product costs. Among various commonly used ESD devices, the silicon-controlled rectifier (SCR) is an excellent candidate due to its very high area-efficiency and robustness [2]. For protecting a pin with an operating voltage ranging between negative and positive values, a dual-directional SCR (DDSCR) can be used to meet the need for providing bidirectional ESD protection as well as reducing area consumption.

Several DDSCRs have been reported in the literature [3] - [7]. A DDSCR was developed by Wang et al. based on BiCMOS technology for the first time [3]. Then an improved DDSCR in the CMOS process was proposed by Vashchenko et al., where heavily doped p+ /n+ regions were inserted to reduce the trigger voltage, but this approach sacrificed the area-efficiency [4]. NMOS structures were introduced into DDSCR by Liu et al. to realize a high area-efficiency and low trigger voltage, but the gates of these devices could suffer latent reliability problems

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[5]. Recently, a segmented DDSCR was proposed by Huang et al. to efficiently elevate its holding voltage [6]. However, the segmentation topology could induce current crowding and thus worsen the ESD robustness. In addition, all of the existing DDSCRs must be implemented in at least three wells and isolated from the P-substrate using additional regions, thus resulting in a large footprint.

In this letter, a compact and self-isolated dual-directional SCR (CSDDSCR) realized in a single N-well is presented. By abandoning the P-well, N-type isolation structure, and any auxiliary trigger module which are normally used in traditional DDSCRs, the proposed structure possesses a very high area-efficiency and excellent overall ESD performance.

II. Device Structure and Operating Mechanism
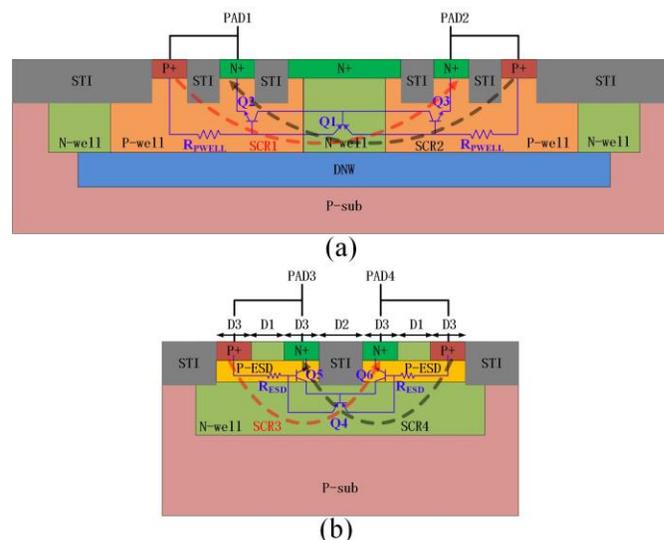
Fig. 1. Cross-sectional view of (a) conventional DDSCR and (b) proposed CSDDSCR.

The cross-sectional view of the conventional DDSCR reported in [4] and the proposed CSDDSCR are shown in Figs. 1(a) and (b), respectively. In the proposed CSDDSCR structure, the P-ESD denotes the p-type ESD implantation available in nanoscale CMOS processes. The P-ESD layer is typically used to improve the turn-on capacity and optimize the current density distribution of the GGNMOS [8]. Recently, this P-ESD implantation is also utilized to enhance the ESD robustness of PMOS and realize vertical SCR structures [9-12], where it serves to isolate the n-type active area from the N-well region and form a vertical N-P-N transistor through the n-type active area (i.e. emitter region), P-ESD layer (i.e. base region) and

N-well (i.e. collector region). In this paper, two of the vertical N-P-N transistors (i.e. Q5 and Q6 in Fig .1(b)) give rise to the proposed CSDDSCR structure by having a common collector region and forming a new lateral P-N-P transistor (i.e. Q4 in Fig .1(b)). The base and emitter electrodes of the N-P-N transistors are connected.

Compared to the conventional DDSCR in Fig. 1(a), the novel CSDDSCR can be realized in only one N-well region, which is self-isolated from the P-substrate. As a result, the two P-well regions and the complicated N-type isolation structure which typically consists of the Deep N-well (DNW) region and the overlapped N-well ring can be dropped. Moreover, unlike the DDSCR which reduces its trigger voltage by forming additional N+/P-well junctions, the CSDDSCR doesn't need any trigger assisted module, as the intrinsic high current gain of the vertical N-P-N transistors (Q5 and Q6) can give rise to a low trigger voltage. All the above-mentioned features make the CSDDSCR device very compact and attractive for ESD applications.

When the PAD3 of CSDDSCR is subject to a positive ESD pulse and PAD4 grounded, the base-collector junction of Q6 is reverse-biased to avalanche breakdown. The generated holes will flow toward PAD4 and will increase the potential of the base region of Q6 and finally turn on Q6. On the other hand, the generated electrons will flow toward PAD3 and will turn on Q4. Consequently, the SCR3 with a low-resistance path (red dash lines in Fig. 1) is created to discharge the ESD current. The same mechanism applies to a reverse mode ESD event where the SCR4 (black dash lines in Fig. 1) takes place. The forward and reverse conduction modes of CSDDSCR possess the same I-V characteristics due to its symmetric structure.

I. RESULTS AND DISCUSSIONS

The novel CSDDSCRs have been fabricated in a 55-nm 3.3v/5v CMOS process with the same device width of 50um. The ESD characteristics were measured using Hanwa TED-T5000 TLP (10ns rise time, 100ns pulse width) and Hanwa HED-T5000VF VFTLP (200ps rise time, 10ns pulse width). The detail measurment results will be discussed below.

A. ESD design window

In order to determine the ESD design window's upper limit, three 3.3v MOS capacitors with different gate lengths have been fabricated in the same 55-nm process and their gate oxide breakdown voltages (BV) have been charcterized using the TLP and VFTLP. Table I summarizes the gate-oxide breakdown voltages of the three 3.3v MOS capacitors. Since the VFTLP has a shorter pulse than the TLP, larger breakdown voltages were obtained under the VFTLP stresses. It was also

TABLE I
MEASURED TLP AND VFTLP BREAKDOWN VOLTAGE OF THE 55-NM 3.3V MOS CAPACITORS. THE FINGER WIDTH AND FINGER NUMBER ARE 10 UM AND 10, RESPECTIVELY.

Gate Length (μm)	BV under TLP (V)	BV under vf-TLP
0.28	13.57	16.25
0.50	13.56	15.70
1.00	13.21	15.07

found that the BV under both types of stress dropped slightly with increasing gate length. Based on these data, the upper limit of ESD design window for this 3.3v/5.5v pin, with a 10% margin, could be set at 11.9V.

B. TLP I-V characteristics
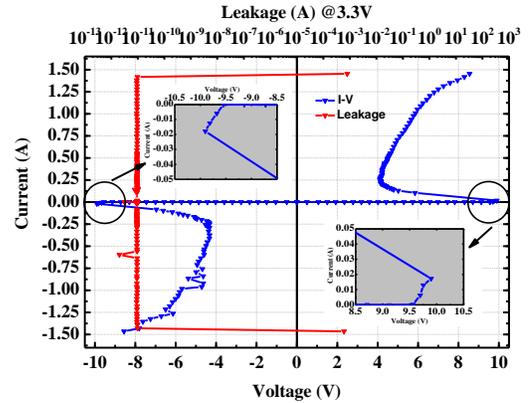
Fig. 2. Measured bidirectional TLP I–V and leakage currents of the proposed CSDDSCR_1.
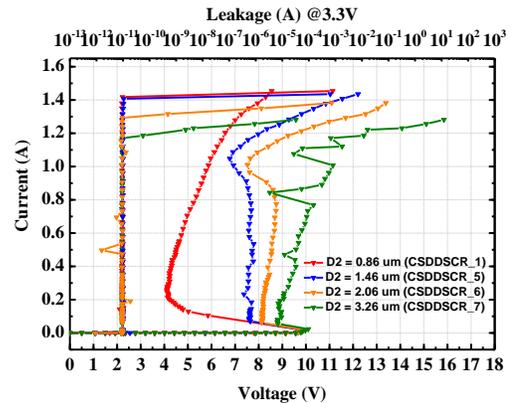
Fig. 3. Measured TLP I–V and leakage currents of CSDDSCR with four different D2.
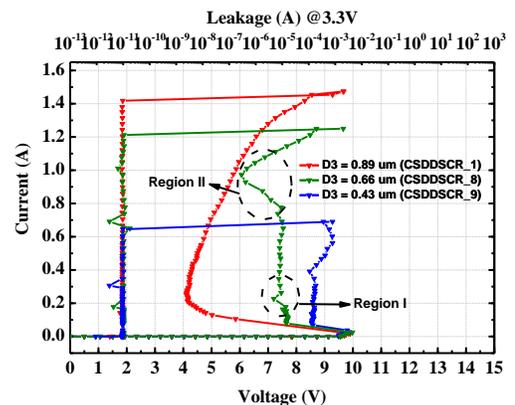
Fig. 4. Measured TLP I–V and leakage currents of CSDDSCR with three different D3.

Measured TLP I–V and leakage currents of the proposed CSDDSCR are shown in Fig. 2, demonstrtaing a symmetrical holding voltage (i.e. V_h) of about ±4 V, trigger voltage (i.e. V_{t1}) of about ±10 V, failure current (i.e. I_{t2}) of about ±1.4 A, and very low leakage current of about 90 pA. These TLP results, together with the deisgn window defined above, have verified

that the CSDDSCR can be used to fulfill the ESD protection requrirements in a 55-nm CMOS process.

Fig. 3 shows the TLP I-V results of CSDDSCRs with four different D2 (the spacing between n+ and n+ regions). Obviously, the holding voltage V_h varies significantly with D2. This results from the low beta in Q4 due to its wide base width. When enlarging D2 from 0.86 to 3.26 um, V_h can be increased from 4.1 to 8.8 V, making it suitable for protecting various input ports in 3.3/5v circuits. However, we must also notice that the failure current I_{t2} drops slightly with increasing D2. As such, D2 should be optimized to efficiently avoid latch-up issue while obtaining high ESD robustness.
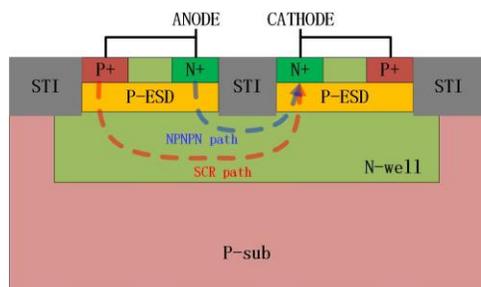
Fig. 5. Current discharge path in the CSDDSCR after second snapback.

(a)

(b)

(c)
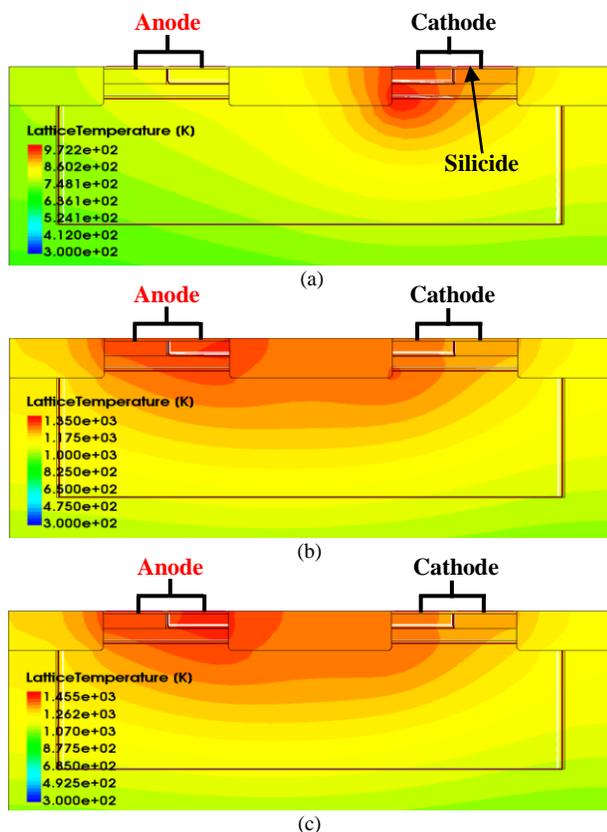
Fig. 6. TCAD simulated lattice temperature distributions of the CSDDSCR_8 at (a) 0.5A (before second snapback), (b) 1.0A (after second snapback) and (c) 1.2A (failure point).

Fig. 4 illustrates the TLP I-V results of the CSDDSCR with different D3 (the width of n+ and p+ regions), demonstrating that V_h is strongly affected by such a dimension. This can be attributed to the deteriorating emitter injection efficiencies in the parasitic NPN (Q3) and PNP (Q1) with reduced emitter

areas when D3 is shrinked, which will require a larger emitter/collector voltage drop, and thus a larger V_h, to maintain the positive feedback state in the SCR. However, the failure current I_{t2} drops sharply with shrunken D3, as the deteriorated current crowding resulting from the smaller emitter area, together with the increased holding voltage, leads to lower It2 results [13]. Nevertheless, as the die area also decreases with the shrink of D3, the ESD robustness per area doesn't correlate with D3 monotonously, acquiring a highest ESD robustness per area of $8.81 \, V/\mu m^2$ with D3 of 0.66 um.

It is indicated that the TLP I-V curves of CSDDSCRs in Fig. 3 and Fig. 4 show multi-triggering characteristics with increment of D2 and decrement of D3, which will be discussed in detail in two cases. As shown in Fig. 4, in the region I, the multi-triggering characteristics is because the elevated holding voltage will worsen the self-heating effect and thus improve the lattice temperature of CSDDSCR, which could eventually increase the ON resistance of the device. However, after each TLP pulse zapping, the actual device temperature may fluctuate due to the influence of the external environment, which will make the ON resistance of the device unstable, thus showing the multi-triggering characteristics in the I-V curve.

In the region II of Fig. 4, the CSDDSCRs show the second snapback characteristics. This is due to the conduction of a new NPNPN path and the inherent current saturation behavior of bidirectional SCR reported in [14]. Considering the anode side of CSDDSCR, as the current goes up, the voltage drop on P-ESD region increases continuously due to the existence of R_{ESD}, which eventually leads to the avalanche breakdown of the reversed-biased N+/P-ESD junction. At this time, a new NPNPN path is created to discharge ESD current along with the original PNPN path, as shown in Fig. 5, resulting in a reduction of the ON resistance and thus the second snapback phenomenon in the CSDDSCR. After the second snapback, the ON resistance of CSDDSCR increases substantially, which is consistent with the current saturation behavior of bidirectional SCR. As shown in Fig. 6(a), before the second snapback, the hotspot in CSDDSCR_8 occurs around the STI region near the Cathode due to the current crowding. However, after the second snapback, the hotspot shifts from the cathode STI to the reversed-biased N+/P-ESD junction because of the latter's avalanche breakdown, which validates that the new NPNPN path is indeed generated in CSDDSCR. Finally, as shown in Fig. 6(c), the device also fails near this N+/P-ESD junction owing to the simultaneous effects of high current and strong electric field.

C. VFTLP I-V and overshoot characteristics

The upper current of the VFTLP measurement is set at 2.5A. Fig. 7 shows the VFTLP I-V curves of several CSDDSCRs with different D2. Consistent with the trend found in the TLP testing, the holding voltage V_h increase monotonically from 3.3v to 5.7v when enlarging D2. Fig. 8 reveals the overshoot characteristics of the CSDDSCRs subject to a current level of 2A. The overshoot voltage of CSDDSCR_1 is much smaller than the DDSCR proposed in [15], which results from the shorter spacing of Anode-to-Cathode (i.e. SAC) used in the CSDDSCR. However, the overshoot voltage dramatically increases from 19v to 40v when enlarging D2 from 0.86 to 3.26 um due to the delay of carrier transport under the transient pulse

[16].
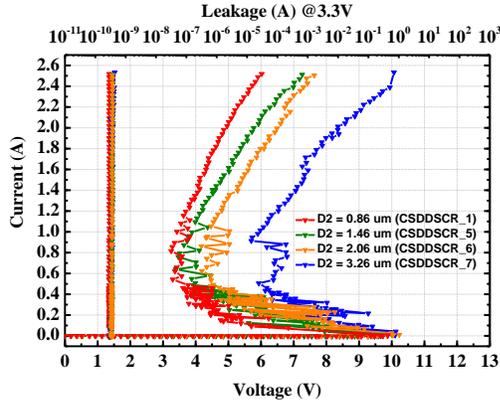
Fig. 7. Measured VFTLP I–V and leakage currents of CSDDSCR with four different D2.
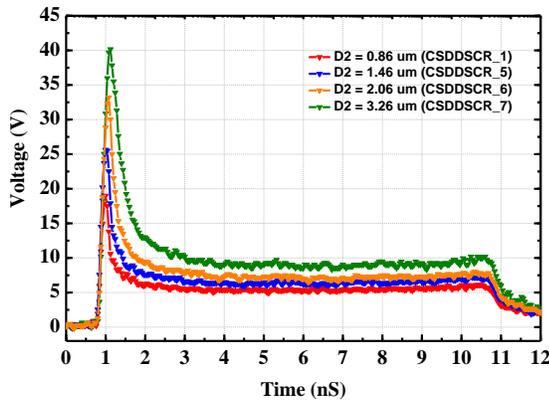
Fig. 8. Measured VFTLP voltage waveforms at 2A of CSDDSCR with four different D2.
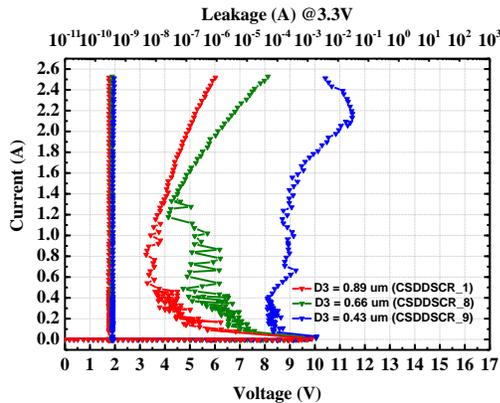
Fig. 9. Measured VFTLP I–V and leakage currents of CSDDSCR with three different D3

Fig. 9 and 10 illustrate the VFTLP I-V and V-t results of CSDDSCRs with different D3, respectively. When decreasing D3, V_h increases significantly from 3.3v to 8v, and the overshoot phenomenon degrades slightly due to a shorter SAC. It is observed that the VF-TLP curves in Fig. 10 have the upward tail with different D3. This is owing to the self-heating effect in the CSDDSCR. For the device (i.e. CSDDSCR_9) subject to a TLP stress close to its failure point, the lattice temperature will increase significantly with the time of pulse action, leading to a larger ON resistance and thus a greater

pressure drop near the end of pulse. On the contrary, For the device (i.e. CSDDSCR_1) subject to a TLP stress away from its failure point, the self-heating effect is not obvious, thus resulting in a gentle tail.
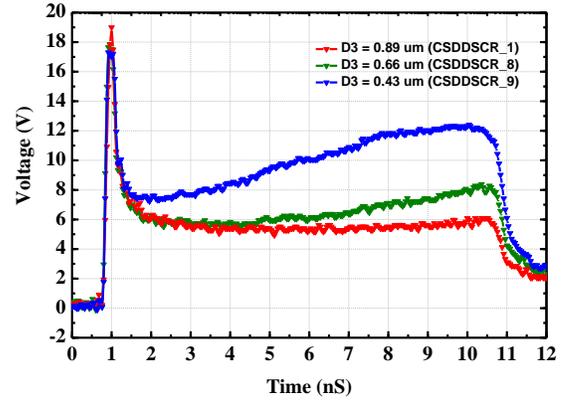
Fig. 10. Measured VFTLP voltage waveforms at 2A of CSDDSCR with three different D3.

D. DC leakage current characteristics

To evaluate the leakage current, bidirectional DC sweeps of CSDDSCR_1 at different temperatures were measured. As shown in Fig. 11, the leakage characteristics of the CSDDSCR are superior, as such a current can still be maintained at a relatively low level when the temperature rises to 125 °C.
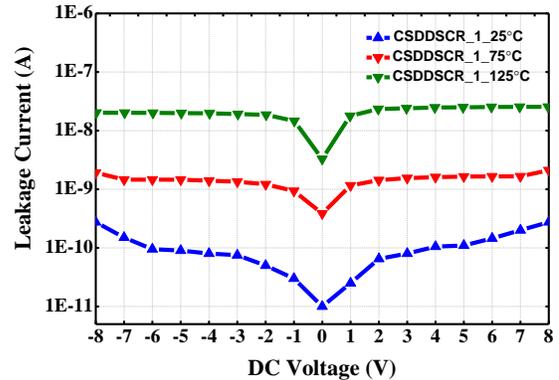
Fig. 11. DC sweep I-V curves of CSDDSCR_1 at different temperatures

E. Parasitic capacitance characteristics
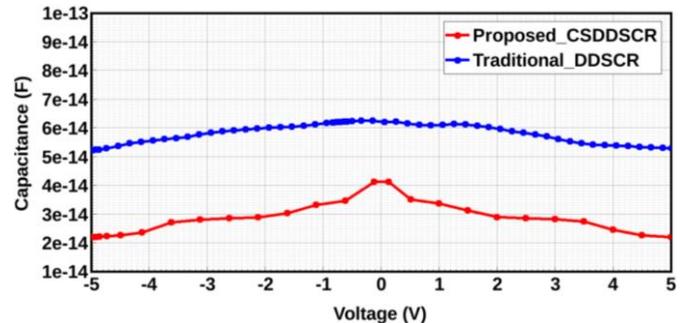
Fig. 12. Simulated parasitic C-V curves at 5GHz for CSDDSCR and DDSCR. The device width of both structures is 50μm.

TABLE II
SUMMARY OF THE LAYOUT PARAMETERS, MEASURED RESULTS AND FIGURE OF MERIT $= V_{HBM}/A \times V_h$.

Device Type	D1 (μm)	D2 (μm)	D3 (μm)	Area (μm²)	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{HBM}/W (V/μm)	V_{HBM}/A (V/μm²)	FOM (V²/μm²)
CSDDSCR_1	0	0.86	0.89	50*5.04	9.90	4.11	1.42	42.6	8.45	34.7
CSDDSCR_2	0.3	0.86	0.89	50*5.64	9.83	3.32	1.54	46.2	8.19	27.2
CSDDSCR_3	0.6	0.86	0.89	50*6.24	9.82	3.30	1.55	46.5	7.45	24.6
CSDDSCR_4	1.2	0.86	0.89	50*7.44	9.98	3.86	1.43	42.9	5.77	22.3
CSDDSCR_5	0	1.46	0.89	50*5.64	9.85	7.38	1.41	42.3	7.50	55.4
CSDDSCR_6	0	2.06	0.89	50*6.24	9.91	8.13	1.32	39.6	6.35	51.6
CSDDSCR_7	0	3.26	0.89	50*7.44	10.1	8.81	1.23	36.9	4.96	43.7
CSDDSCR_8	0	0.86	0.66	50*4.12	9.98	7.20	1.21	36.3	**8.81**	**63.4**
CSDDSCR_9	0	0.86	0.43	50*3.20	9.87	8.55	0.64	19.2	6.00	51.3
DDSCR in [4]	--	--	--	50*42.0	15.5	10.5	3.30	99.0	2.36	24.8
DDSCR in [5]	--	--	--	90*12.5	5.56	2.78	6.13	102.0	8.17	22.7
DDSCR in [6]	--	--	--	50*8.96	15.4	8.30	1.12	33.6	3.75	31.1

TCAD simulation has been carried out to estimate the parasitic capacitances of the CSDDSCR and DDSCR between -5v and 5v at 5 GHz. As shown in Fig. 12, the maximum parasitic capacitance of the CSDDSCR and DDSCR are 41.3 fF and 62.2 fF, respectively. This capacitance reduction is due to the smaller area of the P-ESD/N-well junction used in the CSDDSCR. It should be pointed out that the parasitic capacitance can be further optimized by reducing the dimension of D3.

F. Comprehensive evaluation

We now define the following figure of merit (FOM) to evaluate the overall performance of bidirectional SCRs in terms of ESD robustness, holding voltage and device area:

$$\text{FOM} = V_{HBM}/A \times V_h \qquad (1)$$

where A is the SCR area and V_{HBM} is the HBM passing voltage. Table II summarizes the layout parameters and measured results of several CSDDSCRs and previously reported DDSCRs, where V_{HBM}/A and V_{HBM}/W represents the measured HBM level per area and per device width, respectively. As shown in Table II, on one hand, V_{HBM}/W of CSDDSCRs are relatively inferior to those of the previous DDSCRs proposed in [4] and [5] but a little better than the segmented DDSCR presented in [6]. On the other hand, CSDDSCRs have a distinct advantage over the other devices in terms of V_{HBM}/A. Of all devices considered, CSDDSCRs can also offer relatively high V_h to avert latch-up threat. The CSDDSCR_8 devce has the highest FOM of 63.4 $V^2/\mu m^2$.

II. HOLDING VOLTAGE REVERSAL EFFECT

Another way to optimize the holding voltage of CSDDSCR is to adjust the length of D1 (the spacing between the n+ and p+ regions). However, as shown in Fig. 13, when enlarging D1, V_h decreases initially and then increases. We will call this the holding voltage reversal (HVR) effect. In the following, Sentaurus TCAD simulations will be carried out to further

examine this observation.

Fig. 14 reveals the current density distributions of CSDDSCR and DDSCR, respectively, simulated at a high current level. Both of these devices have two discharge paths at the anode side (i.e., Emitter path and Base path) and two discharge paths at the cathode side (i.e., SCR path and PNP path). On one hand, considering the cathode side, magnifying D1 will depress the current flow via the PNP path while boost the parallel SCR path, resulting in a lower V_h for both CSDDSCR and DDSCR. On the other hand, considering the anode side, the emitter path and base path represent the branch currents via the emitter and base regions of the parasitic PNP transistors (Q4 or Q1), respectively. Notice that the major discharge path at the anode part of the CSDDSCR and DDSCR are different. This is due to the profile differences of the emitter region of the parasitic PNPs where a thinner ESD implantation-type emitter region in the CSDDSCR provides a much larger lateral resistance and a much smaller vertical resistance. Therefore, enlarging D1 equivalently increases the effective base width as well as deteriorates the current gain of parasitic PNP (Q4) in the CSDDSCR, while it equivalently magnifies the emitter resistance of parasitic PNP (Q1) in the DDSCR. Both of these effects will increase V_h of the devices. As a result, the cathode-side mechanism influences V_h more significantly and give rises to a small V_h when D1 is relatively small. When D1 increases, the influence of the anode-side mechanism becomes dominant and V_h is increased. This is the so-called holding voltage reversal effect.

All the CSDDSCRs discussed above have a fully silicided active area. To further explore the effect of metal silicide on the performance of the device, the CSDDSCRs with or without silicide block (SAB) layer located between N+ and P+ blocks on the same electrode have been implemented in the same 55-nm CMOS process. Here the CSDDSCR owns a D1 of 0.5um，a D2 of 0.64um, a D3 of 0.99um and a device width of 140um. As shown in Fig. 15, when the silicide between N+ and P+ blocks are shielded by SAB, the V_h and V_{t1} of CSDDSCR is almost unchanged, indicating that silicide has little effect on the
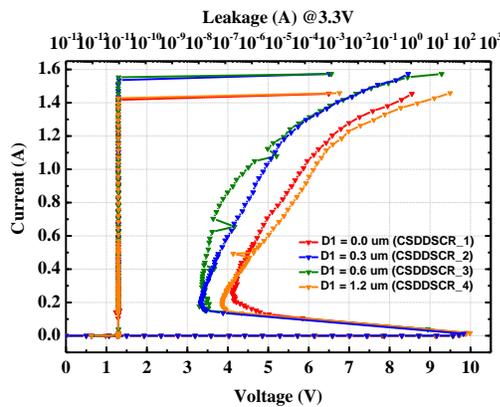
Fig. 13. Measured TLP I–V and leakage currents of CSDDSCR with four different D1.
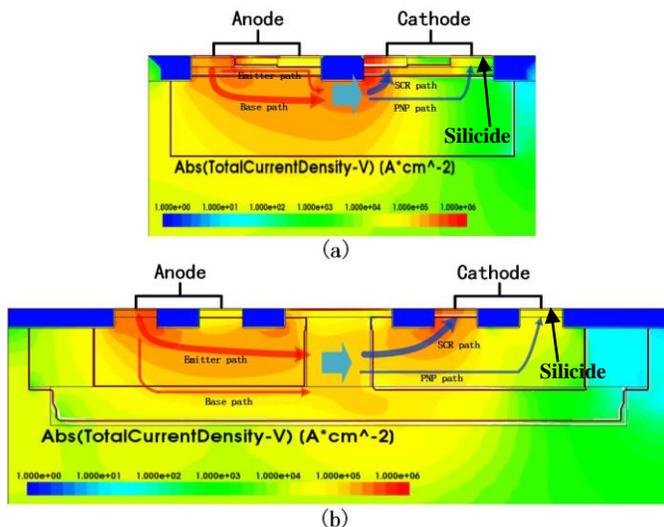
Fig. 14. TCAD simulated current density distributions in (a) proposed CSDDSCR and (b) conventional DDSCR at a current level of 0.5A.
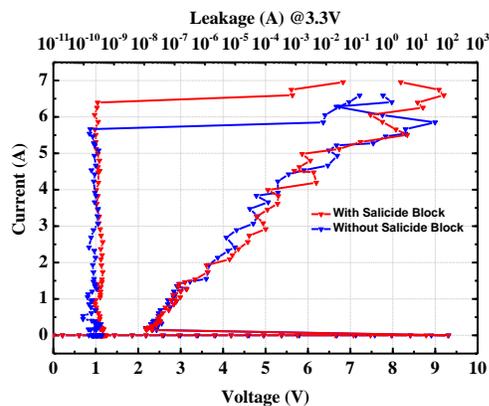
Fig. 15. Measured TLP I–V and leakage currents of CSDDSCR with and without salicide block (SAB). The CSDDSCR here owns a D1 of 0.5um，a D2 of 0.64um, a D3 of 0.99um and a device width of 140um.

current path of CSDDSCR in the triggering and holding stages. This is essentially due to the short connection of N+ and P+ blocks by external metal wires, which is different from [17] where the N+ and P+ blocks in diode structure are connected to different electrodes, respectively. On the other hand, the I_{t2} of the CSDDSCR with SAB is about 1A larger than that of the CSDDSCR without SAB. This may be due to possibility that

the silicide introduced some vulnerable defects on the surface of CSDDSCR, a subject that needs to be studied in more details in the future.

III. CONCLUSION

A novel bidirectional SCR has been proposed and demonstrated. TLP, VFTLP and DC sweep results of the CSDDSCR and previously reported DDSCRs were measured, compared, and discussed. Of all the devices considered, the CSDDSCR illustrates the highest ESD robustness of 8.81 V/μm² and prominent overall performance. A holding voltage reversal (HVR) effect which is universally applicable to all bidirectional SCRs has also been observed and explained with TCAD simulations. Due to the HVR effect, the holding voltage of the DDSCRs needs to be optimized carefully to prevent latch-up risks. An additional mask for ESD implantation may be needed to realize this new structure, hence a slight increase in the cost for fabrication.

IV. ACKNOWLEDGE

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