COURSE SYLLABUS
EE165/EE282D Design for Reliability of Integrated Circuits and Systems

Spring 2026
Dept. of Electrical and Computer Engineering
University of California, Riverside

Instructor:	Prof. Albert Wang	Office:	417 WCH
Phone:	(951) 827-2555	Email:	aw@ece.ucr.edu
Office Hours:	Tuesday 11am – 1pm	Web:	http://www.ece.ucr.edu/~aw
TA:	No		

Course Description:	Covers essentials of electrical transient induced failures to integrated circuits (IC) and systems. Addresses basics for different failure and testing models including electrostatic discharge (ESD), etc. Discusses design-for-reliability (DFR) techniques such as ESD protection designs, etc., at IC, module and system levels. Enhances learning with computer-aided-design (CAD) laboratories
Lecture	T/Th, 2:00pm-3:20pm; Rm125, Student Success Center
Labs	Th 5pm-7:50pm
Prerequisites:	EE100A/B or Graduate stand or Instructor Approval
Text & References:	• Practical ESD Protection Design, Albert Wang, IEEE-Wiley, 2022, ISBN: 978-1-119-85042-7 • Selected papers.
Exam:	No
Project:	Topic Reading (presentation 6/2) Design Project (presentation 6/4)
Grades:	Topic Reading 10% + Labs 50%+ Design Project 40%

Topical Outlines & Schedule
(Subject to modification upon progresses)

Weeks	Date	Lectures		**Labs**
1	3/31&4/2		Essentials for electrical transient phenomena, Fundamentals of EOS/ESD/TVS failures to ICs and systems, Comprehensive ESD/TVS testing models, Basics for ESD protection devices, Advanced ESD protection circuits, ESD protection layout design techniques, Technology impacts on ESD protection structures, CAD technique for ESD protection design, TVS and EMI protection design for electronic modules and systems. ESD-circuit co-design techniques	
2	4/7&9			
3	4/14&16			
4	4/21&23			
5	4/28&30	Topic/Project assignment 4/30		Lab-1 (4/30)
6	5/5&7			Lab 2 (5/7)
7	5/12&14			Lab 3 (5/14)
8	5/19&21			Lab 4 (5/21)
9	5/26&28			Lab 5 (5/28)
10	6/2&4	Topic presentation 6/2; Project presentation 6/4		
11	Final	No		