COURSE SYLLABUS
EE165/EE282D Design for Reliability of Integrated Circuits and Systems

Fall 2024
Dept. of Electrical and Computer Engineering
University of California, Riverside

Instructor:	Prof. Albert Wang	Office:	417 WCH
Phone:	(951) 827-2555	Email:	aw@ece.ucr.edu
Office Hours:	Tuesday 1 – 3pm	Web:	http://www.ece.ucr.edu/~aw
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Course Description:	Covers essentials of electrical transient induced failures to integrated circuits (IC) and systems. Addresses basics for different failure and testing models including electrostatic discharge (ESD), etc. Discusses design-for-reliability (DFR) techniques such as ESD protection designs, etc., at IC, module and system levels. Enhances learning with computer-aided-design (CAD) laboratories
Lecture	T/R, 5:00pm-6:20pm (Humanities and Social Sciences, Room 1503)
Labs	Friday 11am-1:50pm (WCH 128)
Prerequisites:	EE100A/B or Graduate stand or Instructor Approval
Text & References:	• Practical ESD Protection Design, Albert Wang, IEEE-Wiley, 2022, ISBN: 978-1-119-85042-7 • Selected papers.
Exam:	
Project:	Topic Reading (presentation 11/26) Design Project (presentation 12/3&5)
Grades:	Topic Reading 10% + Labs 50%+ Design Project 40%

Topical Outlines & Schedule
(Subject to modification upon progresses)

Weeks	Date	Lectures		**Labs**
1	9/26		Essentials for electrical transient phenomena, Fundamentals of EOS/ESD/TVS failures to ICs and systems, Comprehensive ESD/TVS testing models, Basics for ESD protection devices, Advanced ESD protection circuits, ESD protection layout design techniques, Technology impacts on ESD protection structures, CAD technique for ESD protection design, TVS and EMI protection design for electronic modules and systems. ESD-circuit co-design techniques	
2	10/1&3			
3	10/8&10			
4	10/15&17			Lab-1 (10/18)
5	10/22&24			Lab 2 (10/25)
6	10/29&31	Topic/Proj. assign. 10/29		Lab 3 (11/1)
7	11/5&7			Lab 4 (11/8)
8	11/12&14			Lab 5 (11/15)
9	11/19&21			
10	11/26&~~28~~	Topics presentation: 2X No class 11/28		
11	12/3&5	Project presentation 2X		
12	12/9-13	Final week		