Single-electron memory vs. single-electron logic

- Much simpler architecture for memory
- Passive information storage vs. active information processing
- Easier temperature requirements for memory
- Random background charge OK for single-electron memory

Single-electron memory is much simpler for implementation then single-electron logic

Various meanings of “single-electron memory”

- Bit representation by one electron (or few electrons)
- Coulomb blockade for information storage
- Read-out by single-electron transistor
Single-electron or few-electron bit representation?

Advantages
• Fundamental limit
• Lowest energy dissipation
• Storage element as small as one atom
• No charging “tails” Ŷ fast

Disadvantages
• Information destroyed by single leakage event
• Error probability grows linearly with time
• Refreshing impossible

Best case: single-electron storage (using single atoms?!) but extra redundancy (either few one-electron elements in one memory cell or check sums)
Single-electron Fowler-Nordheim tunneling

Probability distribution of floating gate potential after charging (solid line: random background charge, symbols: $q_0 = -e/2$)

Two possible regimes:
- either many electrons ($n > 10$) stored on the floating gate; random background charge OK,
- or one electron; very long retention time for background charge $q_0 = -e/2$

Few-electron (2-10) regime is bad (fluctuations are too large)

Background-charge-compensated SET readout

Nondestructive readout

Destructive readout

SET operates as a switch

signals before and after erase compared

simpler

better SNR, higher $T$
Defect-tolerant architecture based on nanofuses and nanoshorts

Idea: bit line rerouting by blowing nanofuses and activating nanoshorts

Needs reliable single-use nanofuses and nanoshorts (simple devices!)

Works even for low-yield cells:

Calculating capacitance matrix by FASTCAP

Good agreement between theory and experiment

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<th>Cic,t</th>
<th>Cib,t</th>
<th>Cfi/Cff</th>
<th>Vg period</th>
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<td>8 mV</td>
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<td>ND exp</td>
<td>3.3 aF</td>
<td>0.73 aF</td>
<td>0.2</td>
<td>10 mV</td>
</tr>
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</table>
T-SPICE for SET circuits modeling

Full “orthodox” model for SET is used

J. Yang, T. Gong, and A. Korotkov
T-SPICE modeling results

Resistively-loaded SET inverter

Ring oscillator with three SETs

T-SPICE works for SET circuits, but not very well

J. Yang, T. Gong, and A. Korotkov