

Single-Electron Parametron

KONSTANTIN K. LIKHAREV and ALEXANDER N. KOROTKOV

Department of Physics, State University of New York, Stony Brook 11794-3800

We have suggested a novel family of wireless single-electron digital devices, based on the parametric excitation principle. The basic cell is a short array of small conducting islands separated by tunnel barriers with relatively low capacitance and conductance. External rf (clock) field creates conditions for spontaneous breaking of the charge symmetry of the cell. The symmetry may be broken by the signal field provided by the neighboring cell(s). This mode ensures robust operation of the parametron-based logic circuits. Moreover, these devices may be reversible, dissipating energy well below $k_B T \ln 2$ per logic operation.

Keywords: single-electron digital devices; tunneling; parametron; reversible computation

1. INTRODUCTION

The effects of correlated single-electron tunneling may be used for implementation of ultradense ($n > 100$ Gb/cm²) digital circuits of several types [1]. Circuits based on Single-Electron-Transistor (SET) logic [2] may be close in design to the usual CMOS circuits, but their static power consumption is too high to allow room-temperature operation. This drawback may be avoided in devices of Single-Electron Logic (SEL) [1], which use trapping of single electrons in conducting islands to present digital bits and hence do not have static power dissipation.

Since 1987, several families of SEL devices have been suggested (see Ref. [1] and references therein). In the recently suggested Wireless Single-Electron (WISE) logic [3] which is a SEL-type logic, the necessary energy is supplied by the time-depending electric field $E_m(t)$, which also serves as a global clock. When the field $E_m(t)$ exceeds some threshold value E_p , it induces electric polarization of short one-dimensional arrays serving as basic cells. Field E_s of this

electric dipole may lower the polarization threshold of the neighboring cell and thus pass the data bits electrostatically. However, orientation of fields $E_m(t)$ and E_s is almost the same, leading to small (about 5%) parameter margins.

The goal of this work is to suggest a new version of wireless SEL devices, where perpendicular orientation of the fields $E_m(t)$ and E_s allows more robust operation. As a byproduct of this improvement, the resulting device (which we call Single-Electron Parametron) allows physically-reversible operation, i.e. may be switched between its stable states with dissipation of energy $W \ll k_B T \ln 2$.

2. BASIC CELL

Figure 1a shows a possible implementation of the basic cell of the new family. Three small conducting islands (capacitances $C \ll e^2/k_B T$) form a quasi-linear array, with the middle island slightly shifted out of the axis y . Tunnel barriers with small conductance

($G \ll e^2/h$) allow direct transfer of electrons between the neighboring islands. Let us discuss operation of the cell in the conceptually simplest case when the initially neutral cell is charged by one extra electron. When the clock field $E_m(t)$, which is perpendicular to axis y , is larger than a certain threshold value E_p , it keeps the extra electron inside the middle island (top frame in Fig. 1b). As E_m is reduced below the thresh-

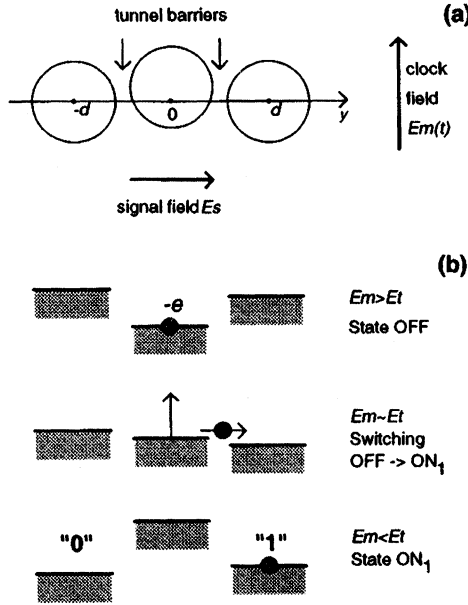


FIGURE 1 Single-Electron Parametron: (a) 3-island version of the device and (b) its energy diagram for three values of the clock field E_m

old, it becomes energy advantageous for the electron to tunnel from the middle island into one of the edge islands, either right or left one. If the system is completely symmetric along axis y , this symmetry breaking is spontaneous, and the direction of the resulting electric dipole moment of the system is random: $P = \pm P_0 n_y$. If, however, the symmetry is broken by some external field E_s with a component along axis y , i.e. by dipole field of a similar neighboring cell, the direction of the electron tunneling and hence of P will be predetermined by this field (middle frame in Fig. 1b). Finally, when E_m is well below E_p , the electron is

well trapped inside one of the edge islands, even if the signal field E_s now favors its transfer into the opposite edge island (bottom frame in Fig. 1b). This transfer may be only achieved via a higher-order tunneling process; probability of this process may be made negligibly small by either decreasing the tunnel conductance or by inserting a few additional islands into the cell [1]. If this parasitic process is suppressed, the cell has a fixed dipole moment and may serve as a source of signal for neighboring cells.

It is evident that the principle of operation of this device is similar to that of the well-known Josephson-junction device called Parametric Quantron (PQ) [4]. The only substantial difference between these devices is that the PQ is described by a continuous degree of freedom (Josephson phase difference ϕ) while the single-electron parametron is characterized by a discrete charge (or the dipole moment P). It is easy to show, however, that both devices share the same basic property: they may operate reversibly. It means that slowly changing external fields may switch the device from one stable state into another adiabatically, with the total energy dissipation much below the apparent limit $k_B T \ln 2$. As a result, the single-electron parametron may be used as a basic cell of reversible computers, provided that their structure supports the informational reversibility (see Ref. [4] and references therein).

Practically, it is more convenient to avoid electric charging of each parametron cell. The device may operate equally well with excitation of electron-hole pairs ("excitons").

3. SHIFT REGISTER

Figure 2 shows a possible structure of a shift register based on single-exciton parametron cells. The axis of the structure (z) is perpendicular to the axis of each cell (y), and is placed into the external clock field $E_m(t)$ of a constant amplitude, rotating in the plane (x, z), and a constant bias field E_b , parallel to axis y . The latter field makes the electrostatic energy of the charge configuration $\text{OFF}_+ = \{-e, +e, 0\}$ equal to that of configuration $\text{OFF}_- = \{0, -e, +e\}$, and the energy of the

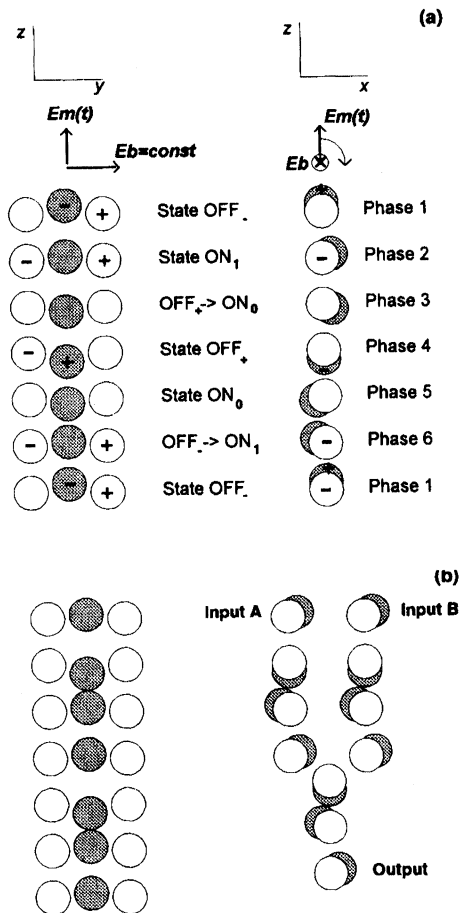


FIGURE 2 Single-electron-parametron-based (a) shift register and (b) two-input gate

configuration $ON_0 = \{0, 0, 0\}$ equal to that of configuration $ON_1 = \{-e, 0, +e\}$. Notice that the electric dipole moments of the cell in these states are substantially different:

$$\mathbf{P}_{ON1} \approx 2\mathbf{P}_{OFF\pm}, \quad \mathbf{P}_{ON0} \approx 0.$$

The middle island of each cell is offset from its axis by the same distance; in each following cell of the structure the direction of this offset is rotated by angle $\pi/3$ within plane (x, z) . As a result, the rotating clock field switches each cell from an OFF state into one of ON states with the $\pi/3$ -phase delay with respect to its upper neighbor. In this moment the upper neighbor is already in a certain ON state, and its field is applied to

the decision-making cell. In the same time, the lower neighbor is still in one of its OFF states with the “neutral” value of P , not affecting the decision. Thus the data bits are propagating from the top to the bottom of the structure, shifted by 6 cells during one clock period.

Our analysis has shown that the single cell may operate correctly within at least $\pm 25\%$ - wide window of the clock field amplitude. Optimization of the shift register as a whole is still in progress, but we expect that it operates reliably within a relatively wide window of basic parameters.

Logic cells may be designed similarly to the shift register. For example, Fig. 2b shows a possible structure of a 2-input logic gate. In this case an additional dc field (parallel to axis y) should be applied to the decision-making cell marked by arrow. The direction of this field will determine the function (OR or AND) performed by this (irreversible) gate. A majority gate (which does not require the additional bias field) and reversible gates of this type [4] may be designed in a similar way.

4. CONCLUSION

We have proposed the logic circuits based on Single-Electron Parametron. This device makes operation of WISE-type logic more robust, and also allows the option of reversible operation.

The work has been supported in part by AFOSR and ONR/ARPA.

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Author Biographies

Konstantin K. Likharev (e-mail: kikharev@ccmail.sunysb.edu) is a Professor of Physics at the State University of New York at Stony Brook. His research interests include digital superconductor electronics, single-electronics, and mesoscopic physics.

Alexander Korotkov (e-mail: akorotkov@ccmail.sunysb.edu) is currently a Research Scientist at SUNY, Stony Brook. His research interests include physics and applications of single-electron tunneling and transport properties of semiconductor heterostructures.