VLSI DESIGN
1998, Vol. 6, Nos. (1-4), pp. 341-344
Reprints available directly from the publisher
Photocopying permitted by license only

© 1998 OPA (Overseas Publishers Association) N.V.
Published by license under
the Gordon and Breach Science
Publishers imprint.
Printed in India.

Analysis of Q_0-Independent Single-Electron Systems

KONSTANTIN K. LIKHAREV and ALEXANDER N. KOROTKOV

Department of Physics, State University of New York, Stony Brook, NY 11794-3800

The random distribution of the background charges is a serious problem for integrated digital single-electron devices with capacitive coupling. We propose the new principle of operation of the devices which does not suffer from this problem.

Keywords: Single-electron tunneling, nonvolatile memories, nanoelectronics

I. INTRODUCTION

Correlated single-electron tunneling [1] is a promising candidate for the physical basis of a new generation of integrated digital devices capable to replace the conventional semiconductor VLSI circuits beyond the 30-nm minimum feature size frontier. However, there are several serious problems on the way to practical integrated single-electronic circuits. Firstly, attempts to directly imitate semiconductor digital circuits by replacing FETs by SETs (Single-Electron Transistors [2]) would lead to relatively large power dissipation at very high integration level ($\sim 10^{11}$ transistors per cm^2) [1-3]. This problem may be circumvented by using one of the Single-Electron Logics [1, 2, 4] where digital bits are presented by single electrons and static power dissipation is negligible. Secondly, in order to avoid thermally induced digital errors, the structures with extremely small capacitance, $C \sim 0.01e^2/k_BT$, and hence of extremely small size should be employed [3]. For room temperature operation, this results in the need of ~1-nm patterning of circuits. Finally, the switching thresholds of digital single-electronic devices are very sensitive to charged impurities trapped in their non-conducting environment [1-3]. For example, a single charged impurity located near a conducting island of the device, may shift its background charge Q_0 by $\Delta Q_0 \sim e$, while the switching thresholds are e-periodic functions of Q_0.

The objective of the present work is to suggest Q_0 insensitive single-electronic devices which may allow the last problem to be avoided, and also facilitate fabrication of the single-electron circuits by softening size requirements by a factor of ~5 (i.e. allowing ~5 nm minimum feature size for room-temperature operation).

II. THE OPERATION PRINCIPLE

The basic idea of the Q_0-independent operation of the capacitively-coupled single-electron transistor is demonstrated in Fig. 1. The "source-drain" current I through the transistor is a e-periodic function of $Q_0+C_gU_{in}$, with amplitude $\Delta I \sim eG/C$, where G and C are the tunnel junction conductance and capacitance, respectively, while C_g is the gate capacitance. The randomness of the background charge Q_0 makes the device response to small signals ΔU_{in} unpredictable. Let us consider, however, a ramp-up of U_{in} by $\Delta U_{in} > e/C_g$. The transistor response will be an oscillation of

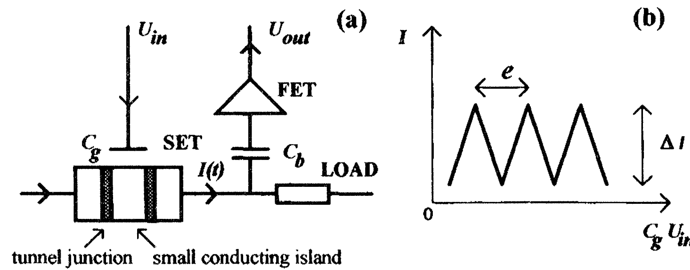

FIGURE 1 (a) SET-FET transistor system and (b) transfer function of the single-electron transistor (schematically)

the current I with *the full swing equal to* ΔI, *regardless of* Q_0. After amplification (say, by a FET sense amplifier) this response may be rectified and serve as the output signal U_{out}. In order to prevent its contamination by the Q_0-dependent dc background, a blocking capacitor C_b may be used between the SET and FET stages (Fig. 1a). In contrast to the logic circuits based on SETs [3], our devices do not require the voltage gain by SETs. This considerably increases the maximal operation temperature: a reasonable modulation of the I - U_{in} dependence is achieved up to $k_BT \sim 0.1e^2/C$.

III. ULTRADENSE SET/FET DYNAMIC RAM

As an example of the application of this general concept, consider a non-volatile dynamic RAM combining SET-based cells and FET sense amplifiers (Fig. 2). As in traditional non-volatile semiconductor memories [5], digital bits are stored in the form of electric charge Q of a floating gate. In our case the gate may be extremely small (of the order of 10 nm) and the charge is just a few electrons. The charge may be changed by its injection/extraction via an element with a sharp conduction threshold V_t. We have considered two possible implementations of this element. The simplest option is to use just a graded dielectric layer with Fowler-Nordheim tunneling above V_t [5]. An alternative is to use an Ohmic resistor $R_t >> h/e^2 \sim 10^4\Omega$ in series with a small tunnel junction [1, 2].

The system dynamics is presented by the phase diagram shown in Fig. 2c; in this diagram, each thin horizontal line corresponds to a certain number n of electrons trapped in the floating gate. The writing threshold V_t for the effective voltage $V_{ef}= C_g(V_W - V_b)/C_\Sigma$ may be reached by the application of positive voltage V_D to the word line and similar negative volt-

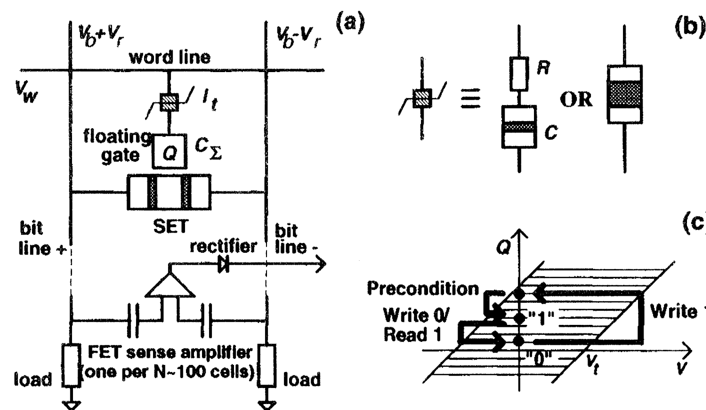

FIGURE 2 Hybrid SET/FET memory: (a) structure, (b) possible threshold elements, and (c) memory cell dynamics shown schematically on its phase diagram

age to both bit lines (C_Σ is the total capacitance of the floating gate). Before readout, the cell is preconditioned by the application of a voltage V_D to the corresponding bit lines (this operation increases parameter margins substantially). Finally, write 0/read operation is achieved by the application of positive $V_b = V_D$ and negative $V_w = -V_D$. The charge of the floating gate changes by $\Delta Q = e\Delta n = -C_\Sigma V_D$, so that the effective charge Q_0 of the SET island changes by $\Delta Q_0 = e\Delta n C_g/C_\Sigma > e$. Because the drain-source voltage $2V_r \sim e/C$ is applied to the transistor simultaneously, its current performs several oscillations (Fig. 1b) during the last process. These oscillations are picked up by a FET sense amplifier (Fig. 2a), which may serve simultaneously a block of $N >> 1$ SET cells connected in parallel (the use of SETs as primary sensors allows the ultrahigh density while FETs provide the voltage amplification). After rectification, this waveform is sent to the output, signaling that the selected cell had the state 1 before the write/read operation; if the state was 0, than $\Delta n = 0$, and no output signal is formed.

Parameter estimates show that the density of 10^{11} bits/cm^{2}and the room-temperature operation can be achieved using 10 nm × 10 nm highly doped Si islands as the floating gates and 4 nm × 4 nm islands as the middle electrodes of SETs. The cycle time is restricted to ~ 3 ns mostly by charge injection to/extraction from the floating gate through a 5-nm graded tunnel barrier with the maximum height of 3.5 eV; processes of charging the SET-FET interconnects (~0.1 ns) and of FET output lines (~1 ns) are considerably faster. The calculation of the intrinsic noise of the SET within the 300 MHz bandwidth shows that even if N = 100 SETs are connected in parallel, the signal-to-noise ratio (~ 10) is still acceptable for a reliable read-out.

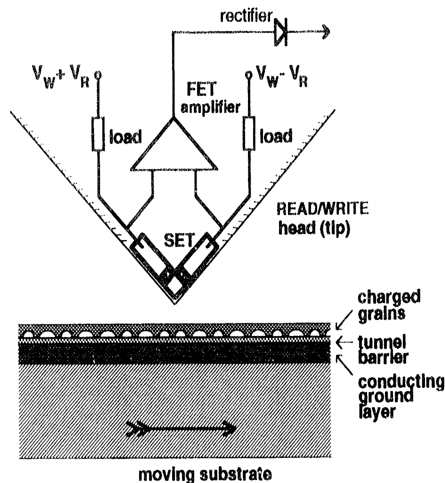

FIGURE 3 Electrostatic storage using SET readout

Another example in which the Q_0-independent operation of the SET could be used, is the data readout from a superdense (up to 10^{12} bits/cm^2) electrostatic storage disk (Fig. 3). Binary data may be written as few-electron charges into the ultrafine conducting grains (~ 1nm) separated from conducting substrate by a ~ 5-nm-thick graded barrier, using the voltage pulse applied to a head (tip) moving close to the surface. Readout of the data may be performed with the same tip carrying the SET/FET transistor pair.

IV. CONCLUSION

We believe that the new Q_0-independent principle of operation of single-electron devices suggested above, and the recent demonstration of silicon-based single-electron transistors with $e/C \sim 0.1eV$ by several groups, may lead to implementation of the first room-temperature single-electron devices in the nearest future.

The work was supported in part by AFOSR and ONR/ARPA.

References

[1] D. V. Averin and K. K. Likharev, "Possible applications of the single charge tunneling", in: *Single-Charge Tunneling,* ed. by H. Grabert and M. H. Devoret, (Plenum, New York, 1992), pp. 311-332.

[2] K. K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions", *IBM J. Res. Dev.,* vol. 32, pp. 144-158, 1988.

[3] A. N. Korotkov, R. H. Chen, and K. K. Likharev, "Possible performance of capacitively coupled single-electron transistors in digital circuits", J. *Appl. Phys.,*vol. 78, pp. 2520-2530, 1995.

[4] A. N. Korotkov, "Wireless single-electron logic", *Appl. Phys. Lett.,* vol. 67, pp. 2412-2414, 1995.

[5] *Nonvolatile Semiconductor Memories*, ed. by C. Hu (IEEE, New York, 1991).

Biographies

Konstantin K. Likharev (e-mail: klikharev@ccmail.sunysb.edu) is a Professor of Physics at the State University of New York at Stony Brook. His research interests include digital superconductor electronics, single-electronics, and mesoscopic physics.

Alexander Korotkov (e-mail: akorotkov@ccmail.sunysb.edu) is currently a Research Scientist at SUNY, Stony Brook. His research interests include physics and applications of single-electron tunneling and transport properties of semiconductor heterostructures.