Single-electron transistor logic

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We present the results of numerical simulations of a functionally complete set of complementary logic circuits based on capacitively coupled single-electron transistors (CSETs). The family includes an inverter/buffer stage, as well as two-input NOR, NAND, and XOR gates, all using similar tunnel junctions, and the same dc bias voltage and logic levels. Maximum operation temperature, switching speed, power consumption, noise tolerances, error rate, and critical parameter margins of the basic gates have been estimated. When combined with the data from a preliminary geometrical analysis, the results indicate that implementation of the CSET logic family for operation at $T \sim 20$ K will require fabrication of structures with ~2-nm-wide islands separated by ~1-nm-wide tunnel gaps.
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The effects of correlated single-electron tunneling (for reviews see, e.g., Refs. 1 and 2) allow the control of the motion of single electrons in solid state structures which consist of conducting ''islands'' separated by tunnel barriers. Regarding digital electronics applications, two ways of exercising this control have been suggested. The first (called ''single-electron logic'', or SEL[3,4]) is to process digital bits in the form of single electrons trapped on conducting islands. In the second single-electron charging is used only inside a specific three-terminal device, the ''single-electron transistor'', or SET.[5,6] From the outside the device looks like the usual transistor, though with its own specific characteristics, and may be used in digital circuits where binary 0 and 1 are represented as usual by two different levels of voltage.[6–9] Despite their considerably higher power consumption,[9] the SET circuits are simpler to implement than SEL circuits, and are the subject of the present analysis.

Earlier, the characteristics of only the simplest buffer/inverter stages of SET logic were analyzed in detail.[9] The results indicate that its characteristics differ considerably from those of their semiconductor FET counterparts, and, therefore, the structure of the logic gates cannot be directly borrowed from CMOS practice. The purpose of this work is to show that, nevertheless, slight modifications allow the natural implementation of several gates forming a complete logic set.

Our calculations were based on the ''orthodox'' theory of correlated tunneling,[1] which is valid when the conductances of all tunnel junctions are small enough: $G \ll e^2/\hbar$. Most results were obtained by numerical modeling of the circuits using the simulation program MOSES.[10]

Figure 1(a) shows the complementary buffer/inverter stage which is structurally identical to that accepted in CMOS technology. The input signal voltage changes the background electrostatic potentials of the middle electrodes of the two SETs and thus the distribution of the bias voltage $2V_B$ across them. The fact that SETs may exhibit negative transconductance allows implementation of complementary circuits using transistors of a single type.[6,7] For performance of multi-input functions, however, direct reproduction of CMOS gates is impossible, because SETs cannot be open in as wide a range of gate voltage as their FET counterparts. As a result, the effective resistance of the SET as a signal source is never too far from its asymptotic (high-voltage) value when the circuit and operation parameters are optimized. Therefore, if we want the high and low levels of output voltage of a gate to be approximately symmetric with respect to

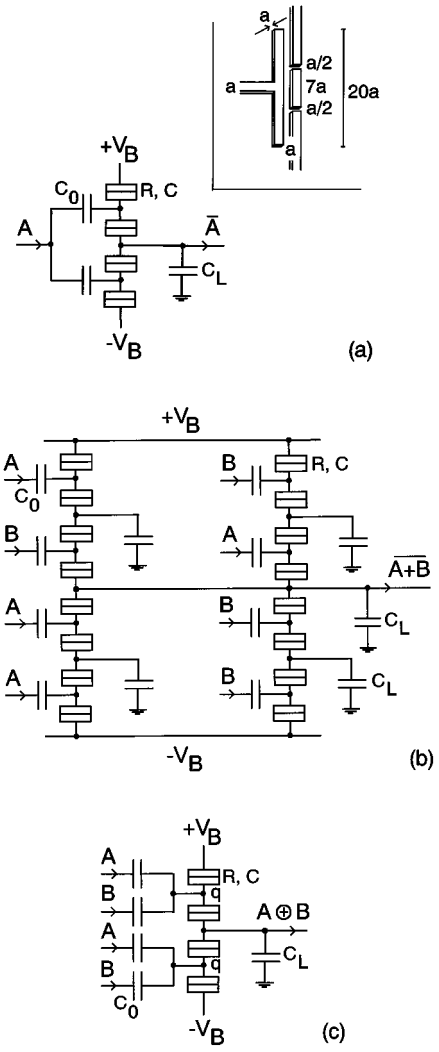

FIG. 1. Basic logic gates of the CSET family: (a) inverter/buffer; (b) NOR; (c) XOR. Vertical flipping of the NOR gate yields a NAND gate with similar performance. Inset in (a) shows the single-electron transistor structure used in our geometrical modeling.

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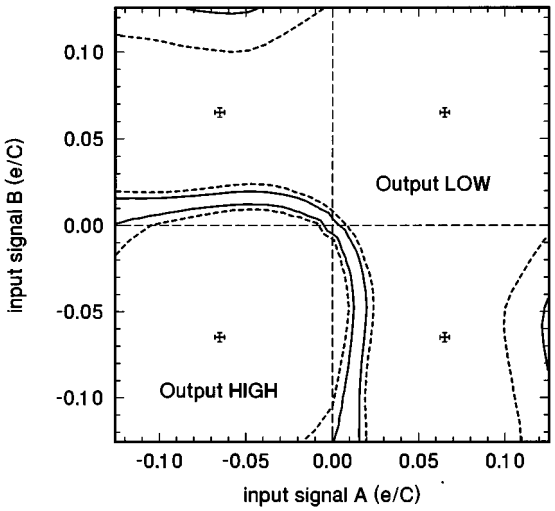

FIG. 2. Output from NOR gate with $C_0/C=3$, $k_BTC/e^2=0.005$ and $V_BC/e=0.125$ on the plane of input signal amplitudes. The solid lines demarcate the active region, where the signal cannot be unambiguously interpreted as either high or low. The areas between solid and dashed lines span the noise margins. Crosses correspond to the nominal amplitudes ($\pm 0.065e/C$).

the ground reference, the asymptotic resistances of its branches on either side of the output terminal should be comparable. A possible structure of a 2-input NOR gate designed along these lines is displayed in Fig. 1(b). Due to the symmetry of the gate and its nominal logic levels, inversion of the dc bias voltage gives a NAND gate with similar characteristics.

In our calculations, the nominal input logic levels were accepted to be equal to the equilibrium values of the inverter; i.e., the values to which signals transmitted through a series of inverters would converge.[9] For the inverter with $V_B=V_0 \equiv e/2(C+C_0)$ ($V_0=0.125\ e/C$ in this case) and the same basic parameters ($C_0/C=3$, $k_BTC/e^2=0.005$) as the NOR gate, they were $\pm 0.065\ e/C$.

Correct operation of the devices requires both that the outputs lie in the allowed range of the appropriate logic level, and that noise tolerance is nonzero. The noise tolerances were calculated in the usual way[11,12] from the transfer characteristics of the inverter/buffer and the NOR/NAND gates biased at V_0. For the above parameters at $k_BTC/e^2=0.005$, the tolerances exceed 20% of the nominal signal value. The inverter and both 2-input gates function correctly when biased with the same voltage V_0 and can sustain bias voltage fluctuations greater than $\pm 50\%$, variations in all coupling capacitances of $\pm 8\%$, and variations in all junction capacitances or tunnel conductances greater than $\pm 40\%$. Performance of the circuits can be even further improved by placing buffer stages between gates. Figure 2 shows the regions of low and high output on the plane of the input signal amplitudes for the NOR gate. One can see that the threshold lines are not too far from the perfect (square) shape.

Another simple gate is the XOR [Fig. 1(c)]. Its output voltage swing is somewhat lower, but it may be made to function correctly within a wide range of V_B by the addition of buffer stages [Fig. 1(a)].

The set of CSET logic gates presented in Fig. 1 is more than sufficient to implement arbitrary logic functions. We have performed an extensive numerical simulation of the gates. The summary of our findings is as follows:

(1) *Maximum operation temperature* for all the devices is $\sim 0.01e^2/Ck_B$, where C is the capacitance of a single tunnel junction, but only at $T\sim 0.005e^2/Ck_B$ do the parameters approach their low-temperature values. Geometric modeling using the FASTCAP package,[13] facilitated by the CONPAN paneling program,[14] has shown that, for a typical SET geometry [Fig. 1(a), inset] $C[\mathrm{aF}]\sim 0.05\varepsilon a[\mathrm{nm}]$.[15] Thus, in order to operate at $T\sim 20$ K the conducting islands formed inside the SiO_2 matrix ($\varepsilon\sim 4$) should have a minimum feature size $a\sim 2$ nm, while being separated by $\sim$1-nm-wide tunnel gaps ($C\sim 0.4$ aF). This spatial pitch ($A\sim 20a\sim 40$ nm per transistor) may allow integrated circuits of an extremely high density ($n\sim 10^{11}$ transistors per cm^2). With recent advances in nanofabrication techniques the implementation of such ULSI circuits may soon be feasible.

(2) *Logic delay* τ of various gates of our CSET family is within the range $(2\text{–}20)C_L/G$, where $C_L \gg C$ is the load capacitance. For a reasonable interconnect length $L=10^2A$[16] we find $C_L/C\sim 2500$. From this estimate, the realistic value $G\sim 3\ \mu\mathrm{S}$ ($\sim 0.1e^2/h$), and the above spatial scale ($a\sim 2$ nm, $A\sim 40$ nm, $L\sim 4\ \mu$m, $C_L\sim 1$ fF) we have $\tau\sim 0.7\text{–}7.0$ ns. This estimate shows that the CSET technology is not spectacularly fast, and can be seen as continuing the speed performance trends of CMOS circuits, though at considerably higher density.

(3) *Reliability* of the CSET gates may be characterized by the rate Γ of digital errors induced by their shot and thermal noise. Our analytical examination and numerical simulations have shown that, for the inverter presented in Fig. 1(a) operating at $T\sim 0.005e^2/Ck_B$ with the parameters above, the output signal crosses the noise margins at a rate estimated as follows:

$$\Gamma \sim \frac{G}{10\sqrt{C_LC}} \exp(-0.031C_L/C), \tag{1}$$

so that for the parameters discussed above the rate is rather low: $\Gamma\sim 10^{-24}\ \mathrm{s}^{-1}$.

(4) The degree of *bidirectionality* may be measured by the change in input potential due to a change in signal applied to the output of the same gate. For our CSET gates $\partial V_{\mathrm{in}}/\partial V_{\mathrm{out}}\sim 2C/C_L \ll 1$, so that bidirectionality is negligible.

(5) *Power consumption* P of the CSET gates shown in Fig. 1 is of the order of $3\times 10^{-3}\ e^2G/C^2$ per SET. For the set of parameters discussed above, $P\sim 10^{-9}$ W per transistor, so that, in order to implement the transistor density $n\sim 10^{11}$ cm^{-2} with all transistors activated continuously, the heat removal capability required is ~ 100 W/cm^2. This figure is some 30 times larger than the natural heat removal rate at this temperature,[17] so some artificial circulation of the cryocoolant may be necessary. A considerable reduction of P is possible using SEL devices.[3,4]

(6) *Background charge variations* may be the largest problem on the road to practical ULSI CSET circuits. In fact, the critical margin in most single-electron devices, including those shown in Fig. 1, is that for the background charge. For our devices the margin is $\Delta Q_0\sim 0.03e$, for background

charge configurations with the same magnitude $|Q_0(i)| = Q_0$ on all transistor islands i. This is much smaller than the rms of random variations of Q_0 in typical present day experiments with relatively large devices ($a \sim 100$ nm). However, several experiments with smaller metallic islands[18–20] can be explained only assuming that $(\delta Q_0)_{\rm rms} \ll e$. Theoretically, this fact can be understood as the result of image charge forces attracting the charge impurities to the surface of the conducting islands, where they induce no background charge.[1] There is a clear need for more experimental studies of these effects for very small conducting particles embedded in various dielectric materials. To a large extent results of these studies may decide the future of CSET digital technology.

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